Data Sheet

BIT1628A

10-Bit Digital Video Decoder With OSD

Version: A1

在接觸此份文件之任何內容以前，請詳細閱讀下開聲明。一旦此份文件揭露予接收者，該接收者即被推定爲同意下開聲明。

Preliminary

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1 General Description

BIT1628A is a high performance digital video decoder combining OSD within one single device. The decoder transfers and decodes most popular NTSC/PAL/SECAM video contents from a video signal source. Signal feeding into BIT1628A includes analog CVBS formats. The Automatic Gain Control (AGC) of A/D converter extends the capability for handling weak and distorted signals. The outstanding 2D comb filter and advanced CTI and Skin-Tone processing improve the display color more clear and more nature of picture quality. Programmable brightness, contrast and color saturation with embedded GAMMA correction let user freely adjust the color of display. Embedded OSD makes system designer very easy to develop a friendly interface between user and end-product. Advanced wide range display format controller can convert a 4:3 display to 16:9 very smoothly. BIT1628A can be used for a traditional hand-held LCD monitor very easily. With the outstanding video processing performance, it is also suitable for Car TV/navigation system and portable AV system.

2 Features

General:

- No external memory required
- One 10-bit video CMOS Analog-to-Digital Converters (ADCs) in differential CMOS style for best S/N-performance
  Fully programmable static gain or automatic gain control (AGC): 0~12db (Analog) and 0~18db (Digital)
- One analog inputs
- Automatic Clamp Control (ACC) for CVBS,
- On-chip clock generator
- L-lock system clock frequencies
- Digital PLL for synchronization and clock generation from all standards and non-standard video sources e.g. consumer grade VTR
- Requires only one crystal (24.576 MHz) for all standards
- Automatic detection of 50 and 60 Hz field frequency, and automatic switching between PAL and NTSC standards
- Accepts NTSC (J, M, 4.43), PAL (60, B, D, G, H, I, M, N), and SECAM (B, D, G, K, K1, L) video signal
- User programmable luminance peaking or aperture correction
- Adaptive 3/5-line comb filter for two dimensional chrominance/luminance separation
- PAL delay line for correcting PAL phase errors
- Multi-standard VBI-data slicer including closed caption
- MV copy protection detection
- YUV to RGB color space converting
- Fully programmable zoom-out arbitrary ratio in both horizontal and vertical
- Anamorphic zoom for 4:3 video input to 16:9 display converting
- Embedded brightness, contrast, sharpness and gamma correction
- Embedded Skin-Tone and CTI
- Embedded programmable OSD for user Interface
- Embedded 3 PWM (Pulse Width Modulation) generators for general purpose control
- Embedded IR remote control decoder

Output:

- 3x8 Bits digital output ports (R,G,B)

- Programmable RGB output port order and pin order
- Maximum output pixel frequency 85MHz@ digital output
- Support inverse and frequency adjustment for LCD panel clock
- Support programmable H/V sync. for LCD panel
- Support Delta and Stripe types LCD panel
- Free-run Synchronization mode if sync signal disappeared

Interface:

- Support Two-Wire Serial Interface (TWSI) Bus interface
- Support 24Cxx serial EEPROM Boot 8051 controller

OSD:

- Built-in OSD generator with 128 ROM fonts, 512 mix color
- 3 windows support overlay function
- 2048x12 prgrammable OSD Memory
- Independent zoom ratio x1~x16 for horizontal and vertical direction
- Programmable Vertical Direction Line Space
- Programmable Horizontal Character Space
- Flashing font attribute
- Fringe font attribute
- Transparent overlay for OSD windows

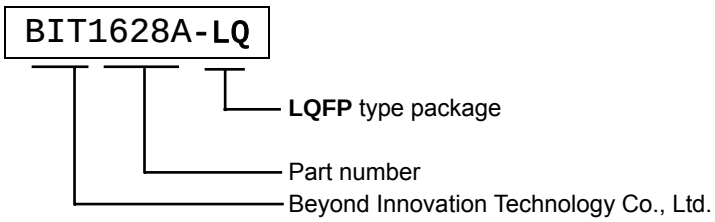
Power management:

- 1.8V power source for core,
- 3.3V power source for output pads
- Power Consumption less than 300 mW

Package:

LQFP 64 pins

3 Order Information



4 Block Diagram

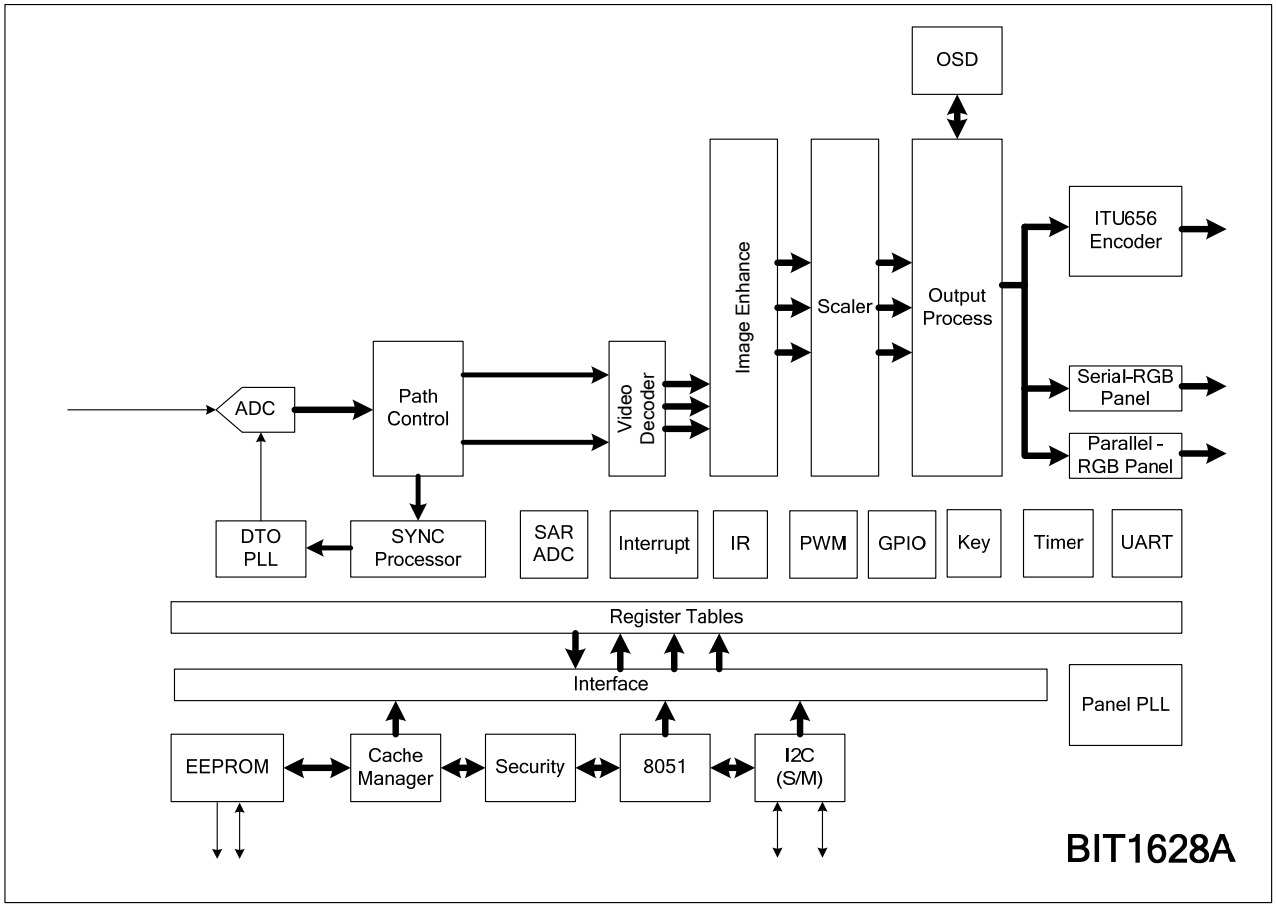


Figure 4-1 BIT1628A Architecture

5 Pin Definition

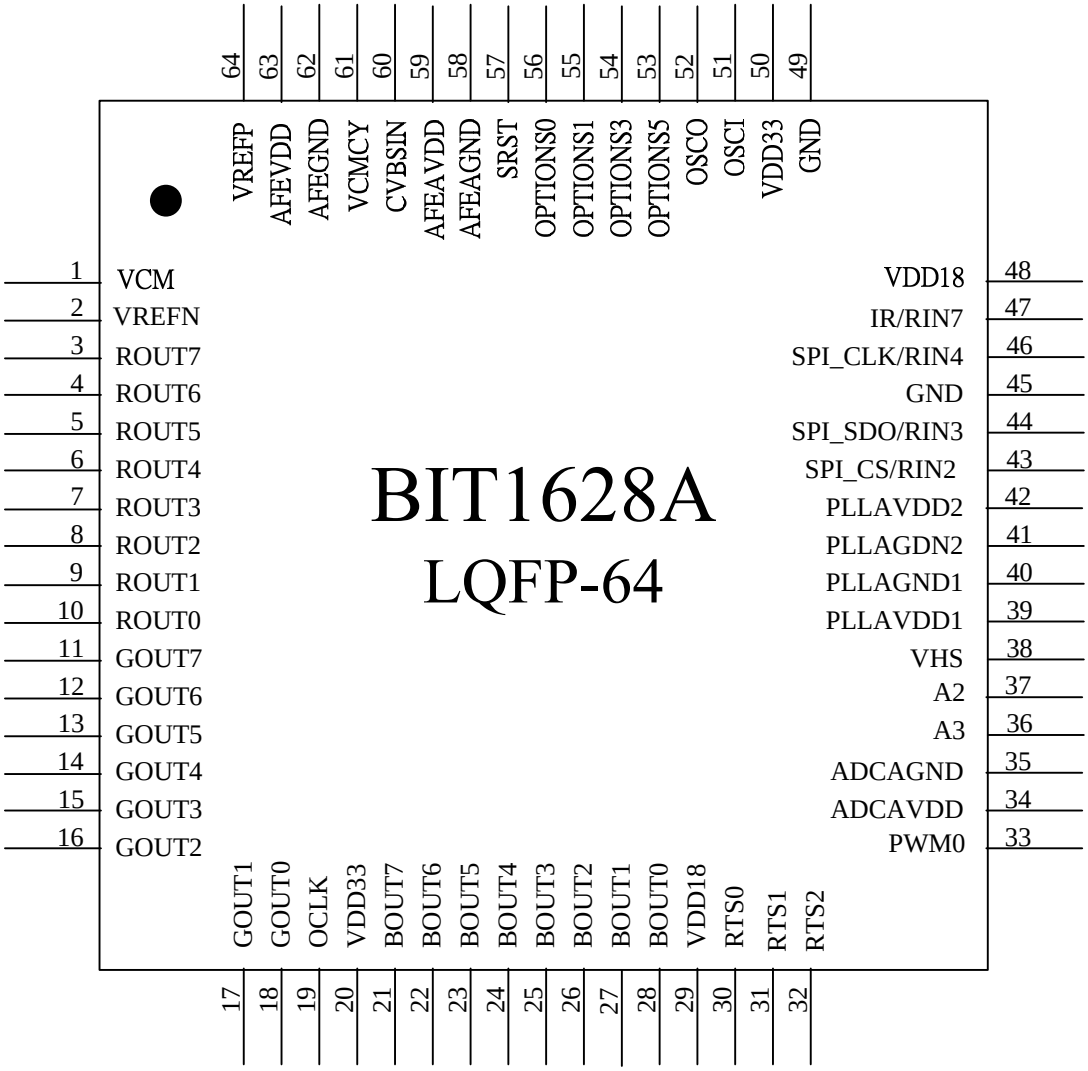


Figure 5-1 Pin configuration

Table 5-1 BIT1628 Pin Definition

Pin Name	Pin #	Pin Type	Function Description	Pad Type
VCM	1	AIO	Output for decoupling or bypass common mode voltage	
VREFN	2	AIO	Output for decoupling or bypass of negative internal reference voltage	
ROUT7	3	O	ROUT[7]	BIO4
ROUT6	4	O	ROUT[6]	BIO4
ROUT5	5	O	ROUT[5]	BIO4
ROUT4	6	O	ROUT[4]	BIO4
ROUT3	7	O	ROUT[3]	BIO4
ROUT2	8	O	ROUT[2]	BIO4
ROUT1	9	O	ROUT[1]	BIO4
ROUT0	10	O	ROUT[0]	BIO4
GOUT7	11	O	GOUT[7]	BIO4
GOUT6	12	O	GOUT[6]	BIO4
GOUT5	13	O	GOUT[5]	BIO4
GOUT4	14	O	GOUT[4]	BIO4

GOUT3	15	O	GOUT[3]	BIO4
GOUT2	16	O	GOUT[2]	BIO4
GOUT1	17		GOUT[1]	BIO4
GOUT0	18		GOUT[0]	BIO4
OCLK	19	O	Clock Output	O16
VDD33	20	P33	IO Power(3.3V)	
BOUT7	21	O	BOUT[7]	BIO4
BOUT6	22	O	BOUT[6]	BIO4
BOUT5	23	O	BOUT[5]	BIO4
BOUT4	24	O	BOUT[4]	BIO4
BOUT3	25	O	BOUT[3]	BIO4
BOUT2	26	O	BOUT[2]	BIO4
BOUT1	27	O	BOUT[1]	BIO4
BOUT0	28	O	BOUT[0]	BIO4
VDD18	29	P18	Core Power(1.8V)	
RTS0	30	O	Multi – Function Output 0	O8
RTS1	31	O	Multi – Function Output 1	O8
RTS2	32	O	Multi – Function Output 2	O8
PWM0	33	O	PWM0 / PPWM0 / IR_SEND	O8
ADCAVDD	34	AP33	SAR ADC Power(3.3V)	
ADCAGND	35	AG33	SAR ADC Ground(3.3V)	
A3	36	AI	SAR A_3 input	
A2	37	AI	SAR A_2 input	
VHS	38	AI	SAR VHS input	
PLLAVDD1	39	AP18	PLL Power (1.8V)	
PLLAGND1	40	AG18	PLL GND (1.8V)	
PLLAGND2	41	AG18	PLL GND (1.8V)	
PLLAVDD2	42	AP18	PLL Power (1.8V)	
SPI_CS/RIN2	43	IO	KEYIN[2] / M8051_P0[2] / SPI_CS	BIO4_UD
SPI_SDO/RIN3	44	IO	KEYIN[3] / M8051_P0[3] /SPI_SDA	BIO4_UD
GND	45	G18	Core Ground(1.8V)	
SPI_CLK/RIN4	46	IO	KEYIN[4] / M8051_P0[4] /SPI_SCL	BIO4_UD
IR/RIN7	47	IO	KEYIN[7] / M8051_P0[7] / IR	BIO4_UD
VDD18	48	P18	Core Power(1.8V)	
GND	49	G	Ground	
VDD33	50			
OSCI	51	I	Crystal Clock Input	
OSCO	52	O	Crystal Clock Output	
OPTIONS5	53	I	Option[5]	I_U
OPTIONS3	54	IO	Option[3]	BIO4
OPTIONS1	55	IO	Option[1]	BIO4
OPTIONS0	56	IO	Option[0]	BIO4
SRST	57	I	Reset	SI_U
AFEAGND	58	AG33	AFE GND (3.3V)	
AFEAVDD	59	AP33	AFE Power (3.3V)	
CVBSIN	60	AI	ADC 1 channel 1 (CVBS)	
VCMCY	61	AI	Luma composite channel PGA negative reference input	
AFEGND	62	AG33	AFE GND (3.3V)	
AFEVDD	63	AP33	AFE Power (3.3V)	
VREFP	64	AIO	Output for decoupling or bypass of positive internal reference voltage	

Table 5-2 PAD Type Definition	
Pad Type	Function
I_U	Input Pad with Pull-up
SI_U	Schmitt trigger input Pad with Pull-up
SI	Schmitt trigger input Pad
O8	8ma Output Pad
O16	16mA Output Pad
BIO4	No Pull-up and Pull-Down Input and 4mA Output Bidirectional Pad Type
BIO4_UD	Programmable Pull-up and Pull-Down Input and 4mA Output Bidirectional Pad Type

6 Functional Description

6.1 System Reset and Power Down Mode

BIT1628A 可以從外部 SRST PIN (Pin 57) 輸入一個大於 16 個 XCLK Cycles 的 Low 訊號，BIT1628 將被強制 Reset 回到 Power On 時的狀態。相關波形請參考 **Figure 6-1**。

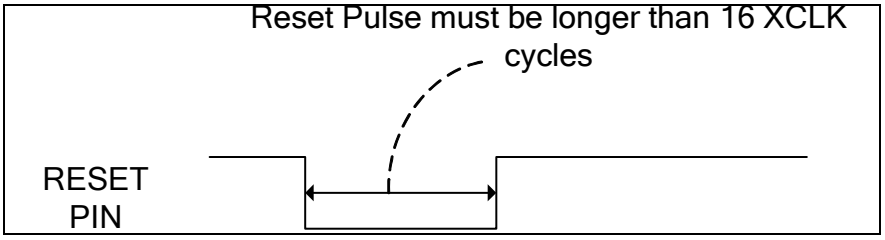


Figure 6-1 Hardware Reset Waveform

6.2 Version Control

BIT1628A 內部提供硬體版本資訊及軟體版本資訊，兩組 Register 作爲版本控管使用，相關 Register 請參考下表。

Table 6-1 Version Control Register

Mnemonic	Address	R/W	Bits	Description	Default
R_HW_VER	0x000	R	8	[1:0] Product version [4:2] Product Number [7:5] Product Group	0xB1
R_SW_VER	0x001	RW	8	Software Version Control	0x00

6.3 Interrupt Function

BIT1628A 內建兩組 Programmable Interrupt Controller (INT0 and INT1),Interrupt Trigger Status 可經由 RTSx PIN (Pin 30,31 and 32),及 Register R_RTSx_SEL 設定爲 0xB(INT0) 0xC(INT1) 輸出(請參考"Special Output Setup"小節的說明)，經由 Register 可設定爲 Edge 或 Level trigger 輸出。當 Level Trigger 時可設定爲 High 或 Low Active，若爲 Edge Trigger 時則可設定爲 Falling 或 Rising Active。其 Interrupt 架構採用三層架構 (FLAG、ACK、MASK)，架構請參考 Figure 6-2。每組 Interrupt 提供 8 個 Interrupt Flags 請參考 Table 6-2，相關 Register 設定請參考 Table 6-3。

在 Master Mode(8051 Mode)時 INT0 and INT1 分別接至 8051 External INT0 and External INT1。

Table 6-2 Interrupt Source and Flags

Interrupt Vector	Interrupt Source 0 (INT0)	Interrupt Source 1(INT1)
[0]	Video Decoder No-Signal	Video Decoder Signal Ready
[1]	Video Processor No-Signal	Video Processor Signal Ready
[2]	Video ADC Value Change Detection	Video Processor Mode Change Detection
[3]	Video Decoder Macrovision Detection	Video Decoder Standard Change Detection
[4]	Video Decoder CC Decoder	Line-Buffer Error
[5]	ADC interface function interrupt	
[6]	IR function interrupt / Slave I2C Interrupt	
[7]	Key function interrupt	

Table 6-3 Interrupt Controller Register					
Mnemonic	Address	R/W	Bits	Description	Default
R_INT0_FLAG	0x002[7:0]	R	8	Interrupt Flag for INT0 0: Nothing. 1: Interrupt event occurs.	-
R_INT0_MASK	0x003[7:0]	RW	8	Interrupt MASK for INT0 (see **Figure 6-2**): 0: Interrupt Mask Off (Enable interrupt). 1: Interrupt Mask On (Disable interrupt).	0x00
R_INT0_ACK	0x004[7:0]	RW	8	Interrupt ACK for INT0 (see **Figure 6-2**): 0: Clear Interrupt Flag and Disable Interrupt. 1: Enable Interrupt.	0x80
R_INT1_FLAG	0x005[7:0]	R	8	Interrupt Flag for INT1 0: Nothing. 1: Interrupt event occurs.	-
R_INT1_MASK	0x006[7:0]	RW	8	Interrupt MASK for INT1 (see **Figure 6-2**): 0: Interrupt Mask Off (Enable interrupt). 1: Interrupt Mask On (Disable interrupt).	0x00
R_INT1_ACK	0x007[7:0]	RW	8	Interrupt ACK for INT1 (see **Figure 6-2**): 0: Clear Interrupt Flag and Disable Interrupt. 1: Enable Interrupt.	0x00
R_ INT0_POL	0x008[0]	RW	1	Interrupt Polarity for INT0 0: High level active (Level Type) 0: Rising edge active (Edge type) 1: Low level active (Level Type) 1: Falling edge active (Edge type)	1
R_INT0_TYPE	0x008[1]	RW	1	Interrupt TYPE for INT0 0: Level Type. 1: Edge Type.	0
R_ INT1_POL	0x008[2]	RW	1	Interrupt Polarity for INT1 0: High level active (Level Type) 0: Rising edge active (Edge type) 1: Low level active (Level Type) 1: Falling edge active (Edge type)	1
R_INT1_TYPE	0x008[3]	RW	1	Interrupt TYPE for INT1 0: Level Type. 1: Edge Type.	0
R_INT_CHT_SEL	0x008[6:4]	RW	3	Video ADC Change Detection enable R_INT_CHT_SEL[0] : AIN11 R_INT_CHT_SEL[1] : AIN12 R_INT_CHT_SEL[2] : AIN2 0: Disable 1: Enable	000
R_ADCINT_TYPE	0x008[7]	RW	1	ADC interface interrupt type 0: Edge trigger 1: Level trigger	1
R_INT0_ISR6_SEL	0x1D4[3:2]	RW	2	Interrupt 6 source select for INT0 00:IR 01: I2C_Slave_TX and I2C_Slave_RX 10: I2C_Slave_TX 11: I2C_Slave_RX	00
R_INT1_ISR6_SEL	0x1D4[5:4]	RW	2	Interrupt 6 source select for INT1 00:IR 01: I2C_Slave_TX and I2C_Slave_RX 10: I2C_Slave_TX	00

				11: I2C_Slave_RX	

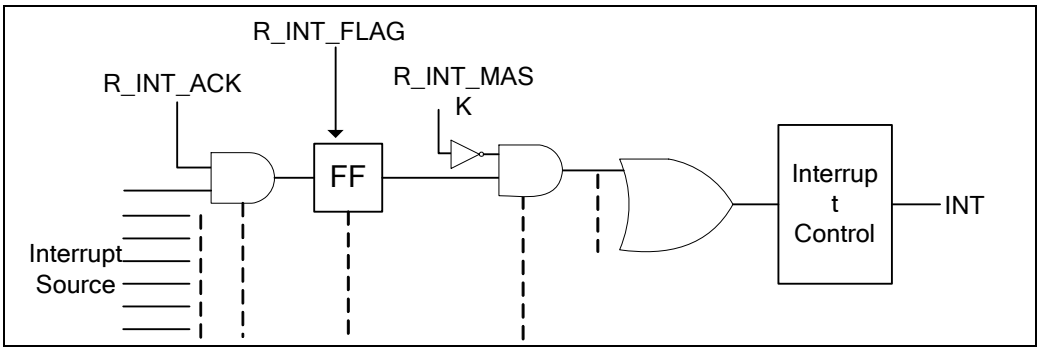


Figure 6-2 Interrupt Function Block

6.4 Clock Domain Systems

BIT1628A 內部存在多組 Clock Domain 相關 Register 設定請參考 **Table 6-4**。

注意事項：XCLK Domain 頻率必須比 LCLK Domain 低。

Table 6-4 Clock Domain System Register

Mnemonic	Address	R/W	Bits	Description	Default
R_LCLK_SEL	0x00B[2:0]	RW	3	LCLK Domain Clock Source Select 000: ICLK1 001: ICLK2 010: PLLCLK 011: OSCCLK 1xx: VDCLK	010
R_LCLK_POL	0x00B[3]	RW	1	LCLK Domain Polarity: 0: Normal. 1: Invert.	0
R_LCLK_EN	0x00B[4]	RW	1	LCLK Domain Enable: 0: Disable. 1: Enable.	1
R_ XCLK_SEL	0x00B[7:5]	RW	3	XCLK Domain Clock Source Select: XCLK = OSCCLK / (2^R_XCLK_SEL)	000
R_CPUCLK_POL	0x00C[0]	RW	1	CPU Mode Clock Polarity 0: Normal 1: Invert	0
R_CPUCLK_EN	0x00C[1]	RW	1	CPU Mode Clock Enable 0: Disable 1: Enable	1
R_TCLK_PRESEL	0x00C[3:2]	RW	2	TCLK Pre-division Factor 00: Division 1 01: Division 2 1x: Division 4	00
R_TCLK_SEL	0x00C[5:4]	RW	2	TCLK Domain Clock Source Select 00: Normal Clock (Freq. equals to Pre-TCLK) 01: Phase 1 Clock (Freq. equals to LCLK/3) 10: Phase 2 Clock (Freq. equals to LCLK/3) 11: Phase 3 Clock (Freq. equals to LCLK/3)	00
R_TCLK_POL	0x00C[6]	RW	1	TCLK Domain Polarity: 0: Normal 1: Invert	0
R_TCLK_EN	0x00C[7]	RW	1	TCLK Domain Enable: 0: Disable 1: Enable	1
R_MCLK_SEL	0x00D[1:0]	RW	2	MCLK Domain Clock Source Select MCLK = PCLK / (R_MCLK_MODE+1)	01
R_MCLK_POL	0x00D[2]	RW	1	MCLK Domain Polarity: 0: Normal 1: Invert	0
R_MCLK_EN	0x00D[3]	RW	1	MCLK Domain Enable: 0: Disable 1: Enable	1
R_ PCLK_SEL	0x00D[5:4]	RW	2	PCLK Domain Clock Source Select: 00: ICLK1 01: ICLK2 1x:VDCLK	00
R_PCLK_POL	0x00D[6]	RW	1	PCLK Domain Polarity: 0: Normal	0

				1: Invert	
R_PCLK_EN	0x00D[7]	RW	1	PCLK Domain Enable: 0: Disable 1: Enable	1
R_DVPCLK_EN	0x00E[0]	RW	1	DVP Clock Domain Enable: 0: Disable. 1: Enable.	1
R_VDCLK_SEL	0x00E[1]	RW	1	Video decoder Clock Select 0: From 27MHz 1: From 13.5MHz	1
R_DVPCLK_POL	0x00E[2]	RW	1	DVP Clock Domain Polarity: 0: Normal. 1: Invert.	0
R_AFECLK_EN	0x00E[3]	RW	1	AFE Clock Domain Enable: 0: Disable. 1: Enable.	1
R_AFECLK_SEL	0x00E[4]	RW	1	AFE Clock Domain Clock Source Select: 0: From 27MHz 1: From 13.5MHz	1
R_AFECLK_POL	0x00E[5]	RW	1	AFE Clock Domain Polarity: 0: Normal. 1: Invert.	0
R_AFEBUF_SEL	0x00E[6]	RW	1	AFE Buffer Clock Domain Clock Source Select: 0: From DVPCLK. 1: From AFECLK	1
R_AFEBUF_POL	0x00E[7]	RW	1	AFE Buffer Clock Domain Polarity: 0: Normal. 1: Invert.	0
R_DVPCLK_SEL1	0x00F[0]	RW	1	DVP Clock Domain 1 Clock Source Select: 0: From DVP Clock Domain 2 1: From AFE Clock Output	0
R_DVPCLK_SEL2	0x00F[1]	RW	1	DVP Clock Domain 2 Clock Source Select: 0: From PLL. 1: From ICLK1	0
R_VDOSCCLK_POL	0x00F[2]	RW	1	Video Decoder OSC Clock domain Polarity 0: Normal. 1: Invert.	0
R_VDOSCCLK_EN	0x00F[3]	RW	1	Video Decoder OSC Clock domain Enable 0: Disable 1: Enable	1
R_REGS_CKEN	0x00F[5]	RW	1	Register Set Power Saving 0: Disable 1: Enable	1
R_OSDCLK_POL	0x00F[6]	RW	1	OSD Clock Domain Polarity 0: Normal. 1: Invert.	0
R_OSDCLK_EN	0x00F[7]	RW	1	OSD Clock Domain Enable 0: Disable 1: Enable	1

6.5 Panel Timing Setup

BIT1628A 可分別針對 Auto Switch 所設定的顯示模式，分爲 Mode 0/1 兩組自動切換 Panel Timing 設定值，其相關設定 Register 請參考 **Table 6-5** 所列，相對應之輸出波形請參考 **Figure 6-3**。

Table 6-5 Panel Timing Setup register					
Mnemonic	Address	R/W	Bits	Description	Default
R_OS_XP	0x013[0], 0x010[7:0]	RW	9	HSYNC Pulse Width	0x00A
R_OS_XS	0x013[1], 0x011[7:0]	RW	9	Active Window Horizontal Start Position	0x025
R_OS_XW	0x013[6:4], 0x012[7:0]	RW	11	Active Window Horizontal End Position	0x345
R_OS_XT_M0	0x016[2:0], 0x014[7:0]	RW	11	Horizontal Total Length on auto switch mode 0	0x4DC
R_OS_XT_M1	0x016[6:4], 0x015[7:0]	RW	11	Horizontal Total Length on auto switch mode 1	0x40D
R_OS_YP	0x017[7:0]	RW	8	VSYNC Pulse Width	0x05
R_OS_YS	0x018[7:0]	RW	8	Active Window Vertical Start Position	0x08
R_OS_YW	0x01B[1:0], 0x019[7:0]	RW	10	Active Window Vertical End Position	0x1E8
R_OS_YT	0x01B[3:2], 0x01A [7:0]	RW	10	Vertical Total Length	0x200

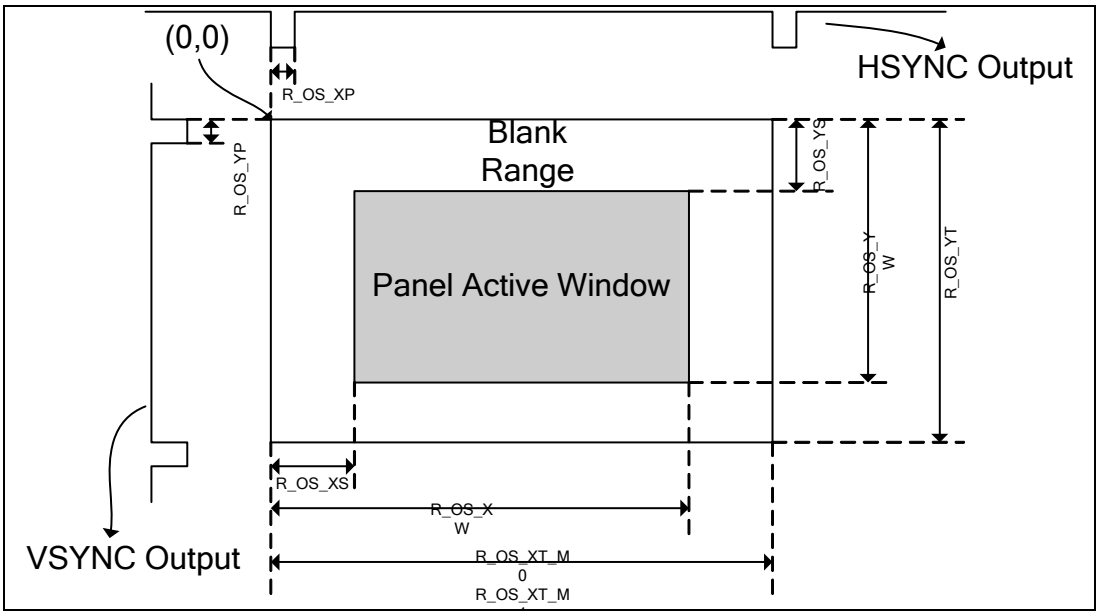


Figure 6-3 Panel Timing Setup

6.6 Special Timing Adjustment

BIT1628A 可針對不同的 Panel Timing 做微調設定，在 Timing 調整上特別提供兩種模式設定，以符合各類 panel 的需求。

6.6.1 Synchronization Timing

在這個模式下的 VSYNC 輸出將會與輸入訊號 VSYNC 同步。

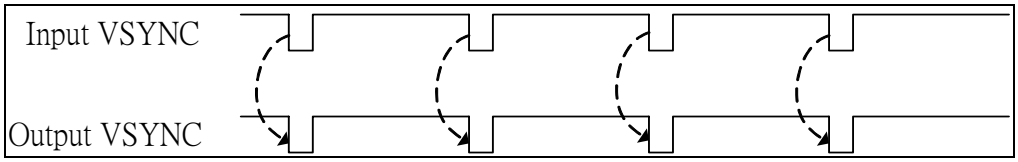


Figure 6-4 Synchronization Timing

6.6.2 Two-Fields Synchronization Timing

在這個模式下的 VSYNC 輸出，將同時受控於所設定欲同步之 EVEN 或 ODD Field VSYNC 和 R_OS_YT (0x01B[3:2], 0x01A[7:0])。

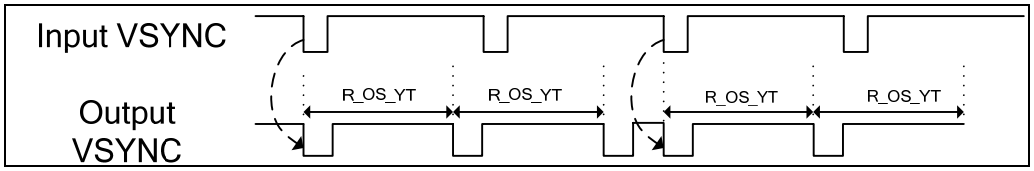


Figure 6-5 Two-Fields Synchronization Timing

其相關設定 Register 及其意義請參考 **Table 6-6**。

Table 6-6 Special Timing Adjust Register

Mnemonic	Address	R/W	Bits	Description	Default
R_PROTECT_MODE	0x01B[4]	RW	1	Minimum Output Lines protection mode 0: Disable 1: Enable	0
R_SYNCO_MODE	0x01B[5]	RW	1	Two-Field Synchronization Mode Select 0: EVEN Field Synchronize 1: ODD Field Synchronize	0
R_SYNCO_EN	0x01B[6]	RW	1	Sync. With input VSYNC enable 0: Two-Field Synchronization Mode 1: Synchronization Mode	1

6.7 Output Data Path

BIT1628A 可針對輸出的 Data Bus 分別做 Invert、Rotate 和 Swap 的處理，其相關設定 Register 請參考 **Table 6-7** ，相對應方塊圖請參考 **Figure 6-6**。

Table 6-7 Output Data Path Register

Mnemonic	Address	R/W	Bits	Description	Default
R_ROL_ROUT	0x01C[1:0]	RW	2	R Data output Rotate	00
R_ROL_GOUT	0x01C[3:2]	RW	2	G Data output Rotate	00
R_ROL_BOUT	0x01C[5:4]	RW	2	B Data output Rotate 00: {D7,D6,D5,D4,D3,D2,D1,D0} 01: {D0,D1,D2,D3,D4,D5,D6,D7} 10: {D2,D3,D4,D5,D6,D7,D1,D0} 11: {D0,D1,D7,D6,D5,D4,D3,D2}	00
R_POL_ROUT	0x01D[0]	RW	1	R Data output Polarity ➔ 0:normal 1:invert	0
R_POL_GOUT	0x01D[1]	RW	1	G Data output Polarity ➔ 0:normal 1:invert	0
R_POL_BOUT	0x01D[2]	RW	1	B Data output Polarity ➔ 0:normal 1:invert	0
R_POL_OCLK	0x01D[3]	RW	1	Output Clock Polarity ➔ 0:normal 1:invert	0

R_SEL_OCLK	0x01D[4]	RW	1	Output Clock Select ➔ 0:LCLK/3 1: LCLK	0
R_SERIAL_MODE	0x01D[7]	RW	1	Serial Mode Enable ➔ 0:Disable 1:Enable	0
R_DLYE_OR	0x01E[1:0]	RW	2	R Channel Output delay n Clock on Swap source = 0	00
R_DLYE_OG	0x01E[3:2]	RW	2	G Channel Output delay n Clock on Swap source = 0	00
R_DLYE_OB	0x01E[5:4]	RW	2	B Channel Output delay n Clock on Swap source = 0	00
R_DLYO_OR	0x01F[1:0]	RW	2	R Channel Output delay n Clock on Swap source = 1	00
R_DLYO_OG	0x01F[3:2]	RW	2	G Channel Output delay n Clock on Swap source = 1	00
R_DLYO_OB	0x01F[5:4]	RW	2	B Channel Output delay n Clock on Swap source = 1 00: delay 1 clock 01: delay 2 clocks 1x: delay 3 clocks	00
R_DLY_MODE	0x01F[7]	RW	1	Delay Mode select 0: normal Mode 1: special Mode (reference from external VCOM)	0
R_SWAPE_OGB	0x020[0]	RW	1	G data output Swap with B data output on Swap source = 0 0: swap disable 1: swap enable	1
R_SWAPE_ORG	0x020[1]	RW	1	R data output Swap with G data output on Swap source = 0 0: swap disable 1: swap enable	0
R_SWAPE_ORB	0x020[2]	RW	1	R data output Swap with B data output on Swap source = 0 0: swap disable 1: swap enable	1
R_SWAPO_OGB	0x020[3]	RW	1	R data output Swap with B data output on Swap source = 1 0: swap disable 1: swap enable	0
R_SWAPO_ORG	0x020[4]	RW	1	R data output Swap with G data output on Swap source = 1 0: swap disable 1: swap enable	0
R_SWAPO_ORB	0x020[5]	RW	1	G data output Swap with B data output on Swap source = 1 0: swap disable 1: swap enable	0
R_SWAP_SRC	0x020[7]	RW	1	Even / Odd Swap source 0: Q2H 1: VCOM	0

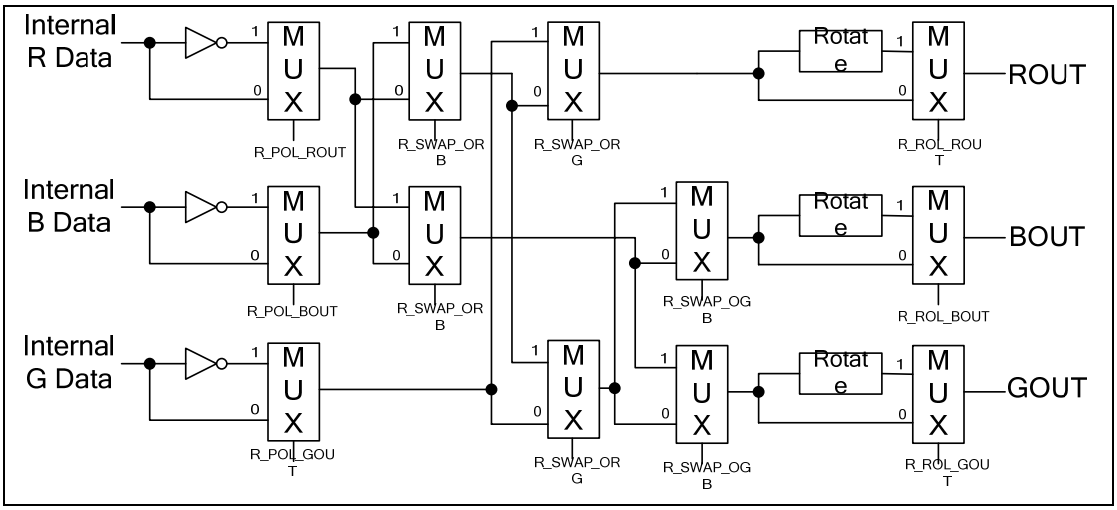


Figure 6-6 Output Data Path Select

6.8 ITU656 Encoder Mode

BIT1628A 內建 ITU656 Encoder 可將影像輸出信號編碼成 8 Bits ITU656 的格式，其相關設定 Register 及其意義請參考 **Table 6-8**。

Table 6-9 ITU656 Encoder Register

Mnemonic	Address	R/W	Bits	Description	Default
R_656ENC_MODE	0x021[1:0]	RW	2	ITU656 Encoder Data Bus Mode Select	00
R_656ENC_HEAD	0x021[2]	RW	1	ITU656 Encoder Handle Enable 0: Disable 1: Enable	1
R_656ENC_EN	0x021[3]	RW	1	ITU656 Encoder Enable 0: Disable 1: Enable	0
R_656ENC_FPOL	0x021[4]	RW	1	ITU656 Encoder F Field Polarity	0
R_656ENC_VPOL	0x021[5]	RW	1	ITU656 Encoder V Field Polarity	0
R_656ENC_HPOL	0x021[6]	RW	1	ITU656 Encoder H Field Polarity 0: Normal 1: Invert	0

6.9 Display Layer

BIT1628A 提供四層 Display Layer 以疊層架構顯示在 Panel 上，高優先權的 Layer 可覆蓋在低優先權的 Layer 相關說明請參考下圖。例如: Layer 5 優先權高於 Layer 4。

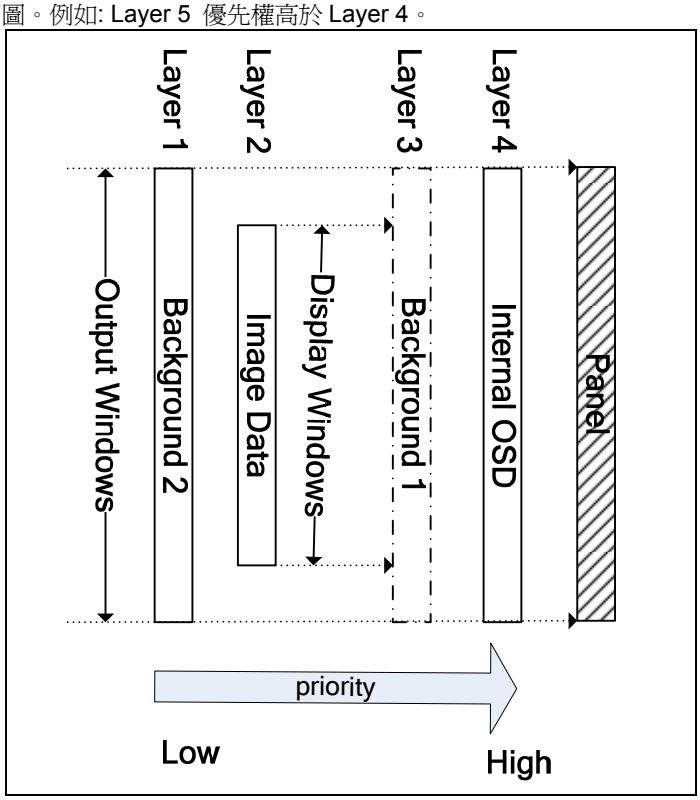


Figure 6-7 Display Layer

6.10 Background 1 and Test Pattern Setup

BIT1628A 內部提供多種內建之 Test patterns 可供選擇，主要分類爲純色、分隔線與漸層(Ramp)及 Color Bar 四種，其相關設定 Register 及其意義請參考 **Table 6-10**。

Table 6-10 Background and Test Pattern Register

Mnemonic	Address	R/W	Bits	Description	Default
R_TESTPAT_R	0x037[5:0]	RW	6	Test Pattern R Color Control value	0x00
R_TESTPAT_G	0x038[5:0]	RW	6	Test Pattern G Color Control Value	0x00
R_TESTPAT_B	0x039[5:0]	RW	6	Test Pattern B Color Control Value R_TESTPAT_TYPE = 00 (Pure Color) [5:0] Test Pattern Color Value R_TESTPAT_TYPE = 01 (Ramp) [5:3] Control Ramp Space R_TESTPAT_TYPE = 10 (Grid) [5:3] Control Grid Space R_TESTPAT_TYPE = 11 (Color bar) [5:0] Color bar color value	0x3F
R_TESTPAT_RATIO	0x3A[5:0]	RW	6	Test pattern Inter count increate ratio	0x3F
R_BACKGROUND_EN	0x03A[6]	RW	1	Background Mode Enable 0: Disable 1: Enable	0
R_FREERUN_EN	0x03A[7]	RW	1	Free-Run Mode Enable 0: Disable 1: Enable	0
R_TESTPAT_TYPE	0x03D[5:4]	RW	2	Test Pattern Type 00: 純色 01: 漸層(Ramp) 10: 分隔線(Grid) 11: Color Bar	01
R_TESTPAT_SUBTYPE	0x03D[7:6]	RW	2	R_TESTPAT_TYPE = 01 (Ramp) 00: Horizontal Ramp 01: Horizontal and Invert Ramp 10: Vertical Ramp 11: Vertical and Invert Ramp R_TESTPAT_TYPE = 10 (Grid) 00: Horizontal Grid 01: Vertical Grid 1x: Horizontal and Vertical Grid R_TESTPAT_TYPE = 11 (Color Bar) 00: Horizontal Color Bar (Space=128) 01: Horizontal Color Bar (Space=64) 10: Vertical Color Bar (Space=128) 11: Vertical Color Bar (Space=64)	00

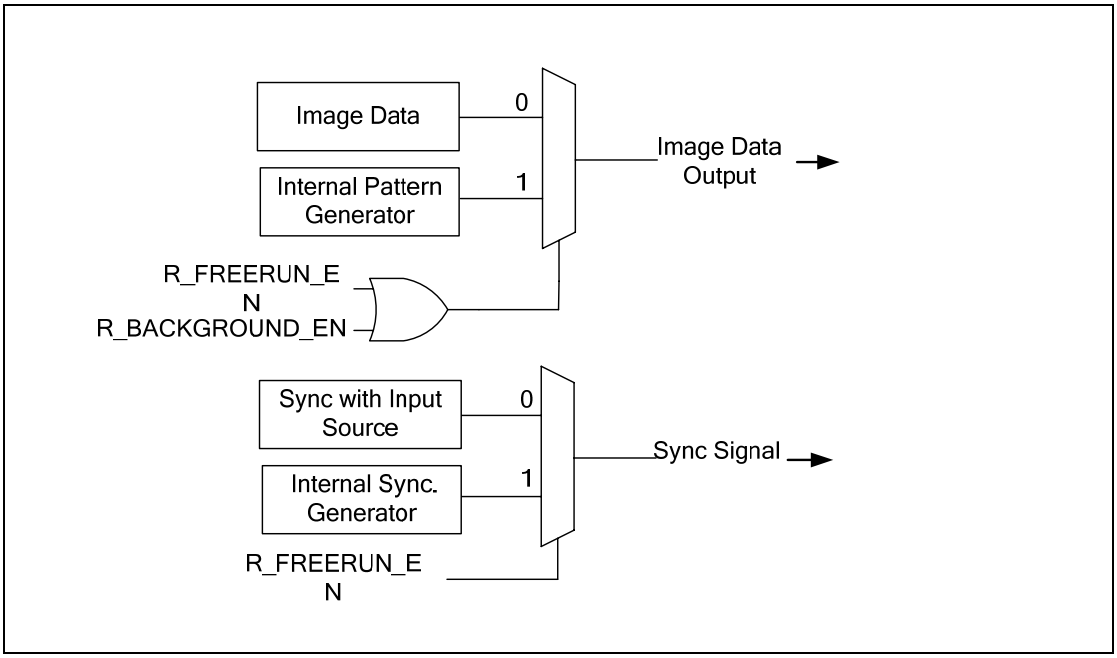


Figure 6-8 Free run and Background

6.11 Background 2

BIT1628A 內部提供 64 種背景色以提供在 4:3 模式下的邊框顯示，其相關設定 Register 及其意義請參考 **Table 6-11**。

Table 6-11 Background 2 Register

Mnemonic	Address	R/W	Bits	Description	Default
R_BG2_R	0x037[7:6]	RW	2	Background 2's R Color used for 4:3 display	00
R_BG2_G	0x038[7:6]	RW	2	Background 2's G Color used for 4:3 display	00
R_BG2_B	0x039[7:6]	RW	2	Background 2's B Color used for 4:3 display	00

6.12 Auto Blank Screen

BIT1628A 內建自動 Blank Screen Function，當訊號中斷或模式切換時將會自動啓動 Blank Screen 畫面，相關設定 Register 請參考下表。

Table 6-12 Blank Screen Register

Mnemonic	Address	R/W	Bits	Description	Default
R_AUTOON_TIME	0x03B[6:0]	RW	7	Blank Screen to Normal Screen Delay times (based on VSYNC)	0x04
R_AUTOON_EN	0x03B[7]	RW	1	Blank Screen Function Enable 0: Disable 1: Enable	0
R_AUTOOFF_TIME	0x03C[4:0]	RW	5	No signal to Blank Screen Delay times(based on Output VSYNC)	0x02
R_AUTOON_MODECHG	0x03C[5]	RW	1	AUTOON Refer Mode change signal	1
R_AUTOON_NOSIG	0x03C[6]	RW	1	AUTOON Refer No signal 0: Disable 1: Enable	1
R_AUTOON_EVEN	0x3C[7]	RW	1	EVEN/ODD Auto gen. when AUTOON 0: Disable 1: Enable	1

R_HLCK_SEL	0x03D[0]	RW	1	HLCK Detection Enable 0: Disable 1: Refer HLCK	1
	0x03D[1]	RW	1	Sync Ready Detection Enable 0: Disable 1: Refer SYNC	0
	0x03D[2]	RW	1	Standard Ready Detection Enable 0: Disable 1: Refer STD	0
R_NOSIG_SEL	0x03D[3]	RW	1	Blank Screen Function Signal Select 0: From VP Signal 1: From VD Signal(R_HLCK_SEL)	0

6.13 Input Image Window Setup

設定 Input Image Window，BIT1628A 將針對此區域內的資料進行 Scaling 運算。其相關設定 Register 請參考 Table 6-13，相對應之示意圖請參考 Figure 6-9：

Table 6-13 Input Crop Register

Mnemonic	Address	R/W	Bits	Description	Default
Auto switch mode 0 input widows setup					
R_IS_XS_M0	0x040[1:0], 0x03E[7:0]	RW	10	Input Window horizontal Start Position	0x09B
R_IS_XW_M0	0x040[7:4], 0x03F[7:0]	RW	12	Input Window horizontal End Position	0x347
R_IS_YS_M0	0x043[1:0], 0x041[7:0]	RW	10	Input Window vertical Start Position	0x014
R_IS_YW_M0	0x043[6:4], 0x042[7:0]	RW	11	Input Window vertical End Position	0x138
Auto switch mode 1 input windows setup					
R_IS_XS_M1	0x046[1:0], 0x044[7:0]	RW	10	Input Window horizontal Start Position	0x09B
R_IS_XW_M1	0x046[7:4], 0x045[7:0]	RW	12	Input Window horizontal End Position	0x346
R_IS_YS_M1	0x049[1:0], 0x047[7:0]	RW	10	Input Window vertical Start Position	0x013
R_IS_YW_M1	0x049[6:4], 0x048[7:0]	RW	11	Input Window vertical End Position	0x103

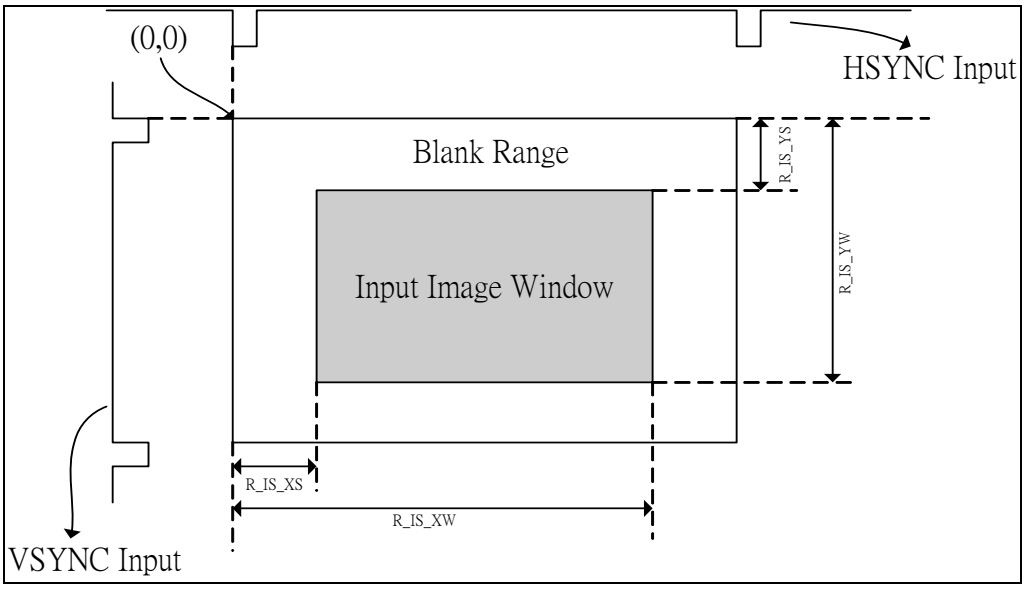


Figure 6-9 Input Window Setup

6.14 Input Data Path Setup

BIT1628A 可針對輸入的 Data Bus 分別做 Invert、Rotate 和 Swap 的處理，其相關設定 Register 請參考 **Table 6-14**，相對應之方塊圖請參考 **Figure 6-10**。

Table 6-14 input Data Path Register					
Mnemonic	Address	R/W	Bits	Description	Default
R_POL_RIN	0x04A[0]	RW	1	R Data input Polarity ➔ 0:normal 1:invert	0
R_POL_GIN	0x04A[1]	RW	1	G Data input Polarity ➔ 0:normal 1:invert	0
R_POL_BIN	0x04A[2]	RW	1	B Data input Polarity ➔ 0:normal 1:invert	0
R_ROL_RIN	0x04A[3]	RW	1	R Data Rotate ➔ 0:disable 1:enable	0
R_ROL_GIN	0x04A[4]	RW	1	G Data Rotate ➔ 0:disable 1:enable	0
R_ROL_BIN	0x04A[5]	RW	1	B Data Rotate ➔ 0:disable 1:enable	0
R_ISWAP_RB	0x04C[0]	RW	1	R Data bus swap B Data bus ➔ 0:disable 1:enable	0
R_ISWAP_RG	0x04C[1]	RW	1	R Data bus swap G Data bus ➔ 0:disable 1:enable	0
R_ISWAP_GB	0x04C[2]	RW	1	G Data bus swap B Data bus ➔ 0:disable 1:enable	0
R_VD_PATH	0x04C[3]	RW	1	Bus Select ➔0: External RGB Port, 1: Internal Video decoder	0

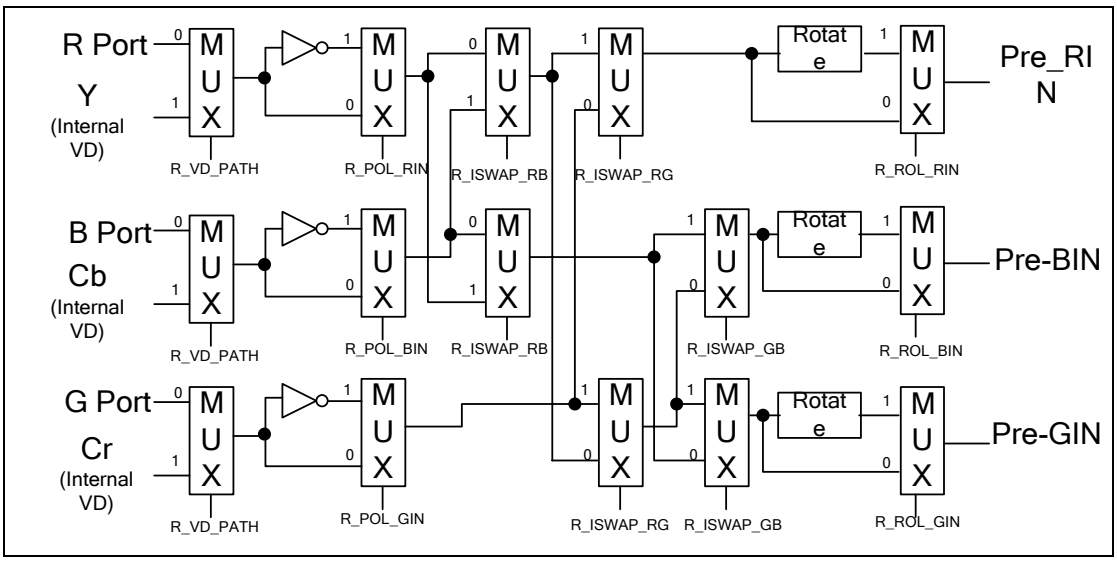


Figure 6-10 Input Data Path Setup

6.15 Input Mode Selection

BIT1628A 經由 Register 設定決定輸入模式，其相關設定 Register，請參考 Table 6-15，相對應之方塊圖請參考下圖。

Table 6-15 Input Mode Select Register

Mnemonic	Address	R/W	Bits	Description	Default
R_IDE_SEL	0x04A[7:6]	RW	2	External Data Enable Source Select 00: External HSYNC pin 01: External VSYNC pin 10: ITU656 HSYNC Signal 11: ITU656 VSYNC Signal	01
R_POL_IDE	0x04B[1]	RW	1	Data enable Polarity 0: Normal 1: Invert	0
R_POL_IHS	0x04B[2]	RW	1	External HSYNC polarity ➔ 0:Normal, 1:Invert	0
R_POL_IVS	0x04B[3]	RW	1	External VSYNC polarity ➔ 0:Normal, 1:Invert	1
R_SEL_EVEN	0x04B[5:4]	RW	2	EVEN/ODD Signal Select 00: ITU656-EVEN Signal 01: Visual EVEN/ODD Signal 10: Always EVEN Field 11: Always ODD Field	01
R_EXT_SYNC	0x04B[7:6]	RW	2	Sync Source Select 00: ITU656 01: Video Decoder 10: External HS/VS 11: Data Enable	00
R_SORT_656	0x04C[6:4]	RW	3	ITU656 / ITU601 Format ➔ Data sequence Shift Control X00: No Shift X01: Shift 1 Clock X10: Shift 2 Clocks X11: Shift 3 Clocks Serial – RGB Format ➔ Serial-Bus Data Sort Control 000: Always 0 001: R-G-B 010: R-B-G 011: G-R-B 100: G-B-R 101: B-G-R 110: B-R-G 111: Always 1 RGB 5:6:5 Format ➔ Data compensation mode X0X: Compensate with R_SORT_656[0]. X1X: Compensate with LSB Data.	000
R_VISUAL_TYPE	0x04C[7]	RW	1	Visual EVEN/ODD Mode 0: Normal EVEN/ODD Mode 1: Always Change by VSYNC	1
R_SRC_SEL	0x04D[1:0]	RW	2	Source Format Select RGB Domain Source ➔ R_IMODE= 1 00: Serial-RGB Format 01: RGB 5:6:5 Format 1x: RGB 8:8:8 Format YUV Domain Source ➔ R_IMODE = 0 00: ITU656 / ITU656-Like Format 01: ITU601 Format	00

				1x: YUV 4:4:4 Format	
R_SWAP_UV	0x04D[2]	RW	1	Swap U and V signal 0: Disable 1: Enable	0
R_IMODE	0x04D[3]	RW	1	Input Mode Select 0: YUV Domain Source Input 1: RGB Domain Source Input	0
R_PCLK_BASE	0x04D[5:4]	RW	2	Input Active Pixel Mode 00: 1-Pixel Mode (RGB888、RGB565、YUV444、ITU601) 01: 2-Pixel Mode (ITU656/ITU656-Like) 10: 3-Pixel Mode (Serial RGB) 11: 4-Pixel Mode	01
R_RGB2YUV_EN	0x04D[6]	W	1	RGB to YUV Color space convert enable 0: Disable 1: Enable	1
R_Y2R_SEL	0x04D[7]	W	1	YUV to RGB Mode Select 0: Gamma correction 1: Non-Gamma correction	0

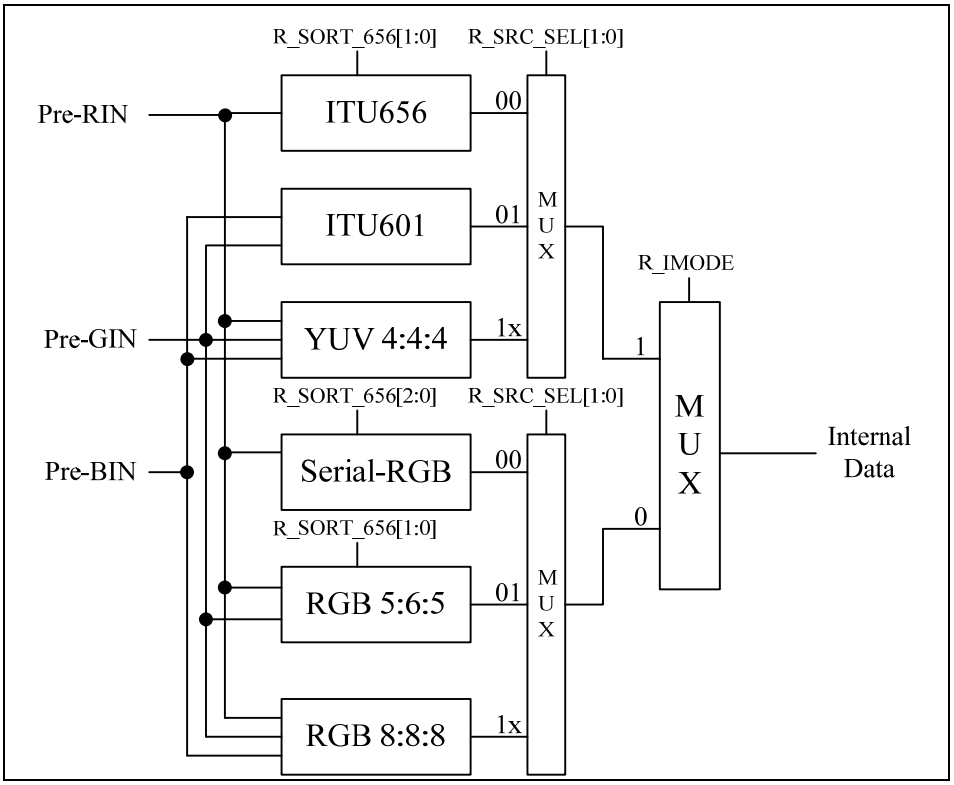


Figure 6-11 Input Mode Select

6.16 Auto Switch

BIT1628A 針對 Input Windows、Vertical Scaling Factor 和 Timing setup 提供兩組 Register 設定，可分別設定爲自動或手動切換模式，當在自動模式時 BIT1628A 將會判別輸入訊號爲 50Hz or 60Hz 自動切換至相對應的 Register 群組，其相關設定 Register 請參考 **Table 6-16**。

Table 6-16 Auto Switch Register

Mnemonic	Address	R/W	Bits	Description	Default
R_AUTO_SWITCH	0x04E[0]	RW	1	Auto Switch Mode 0: Manual Mode 1: Auto Mode	0
R_SWITCH_MODE	0x04E[1]	RW	1	Manual Mode Select 0: Select Mode0 1: Select Mode1	1

6.17 Auto Switch 2

BIT1628A 針對 Display Windows 和 Horizontal Scaling Factor 提供兩組 Register 設定，可分別設定爲自動或手動切換模式，當在自動模式時 BIT1628A 將會判別輸入訊號爲 50Hz or 60Hz 自動切換至相對應的 Register 群組，其相關設定 Register 請參考 **Table 6-17**。

Table 6-18 Auto Switch 2 Register

Mnemonic	Address	R/W	Bits	Description	Default
R_AUTO_SWITCH2	0x04E[2]	RW	1	Auto Switch 2 Mode 0: Manual Mode 1: Auto Mode	0
R_SWITCH2_MODE	0x04E[3]	RW	1	Switch 2 Manual Mode Select 0: Select Mode0 1: Select Mode1	1
R_AUTOSWITCH_SRC	0x04E[4]	RW	1	Auto Switch / Switch2 Source Select 0: Video Decoder FIDT 1: Mode Type	0

6.18 Display Window Setup

BIT1628A 定義了一個 Display Window 的區域，將 Scaling 後的影像資料顯示於此區域內，因此在 Timing 許可下，可任意做上下左右 Move(Pan)和 Resize 的動作，其相關設定 Register 請參考 **Table 6-19**，相對應之示意圖請參考 **Figure 6-12**。

Table 6-19 Display Windows Register

Mnemonic	Address	R/W	Bits	Description	Default
R_PREDIS_ACTX_S0	0x051[1:0],0x04F[7:0]	RW	10	Display Window Pre-Scaling Active Horizontal Width for Switch2 Mode0	0x320
R_PREDIS_ACTX_S1	0x051[5:4],0x050[7:0]	RW	10	Display Window Pre-Scaling Active Horizontal Width for Switch2 Mode1	0x280
R_DIS_XS_S0	0x054[2:0], 0x052[7:0]	RW	11	Display Window Horizontal Start Position for Switch2 Mode0	0x025
R_DIS_XW_S0	0x054[6:4], 0x053[7:0]	RW	11	Display Window Horizontal End Position for Switch2 Mode0	0x346
R_DIS_XS_S1	0x057[2:0], 0x055[7:0]	RW	11	Display Window Horizontal Start Position for Switch2 Mode1	0x075
R_DIS_XW_S1	0x057[6:4], 0x056[7:0]	RW	11	Display Window Horizontal End Position for Switch2 Mode1	0x2F5
R_DIS_YS	0x05A[3:2],0x058[7:0]	RW	10	Display Window Vertical Start Position	0x008
R_DIS_YW	0x05A[1:0], 0x059[7:0]	RW	10	Display Window Vertical End Position	0x1E8
R_DIS_XW1	0x05D[2:0], 0x05B[7:0]	RW	11	Display Window Active Horizontal Width On Linear Mode : Define all region On Anzoom Mode: Define 1 and 3 region	0x320
R_DIS_XW2	0x05D[6:4], 0x05C[7:0]	RW	11	Display Window Active Horizontal Width	0x000

				On Linear Mode: No active. On Anzoom Mode: Define 2 region	

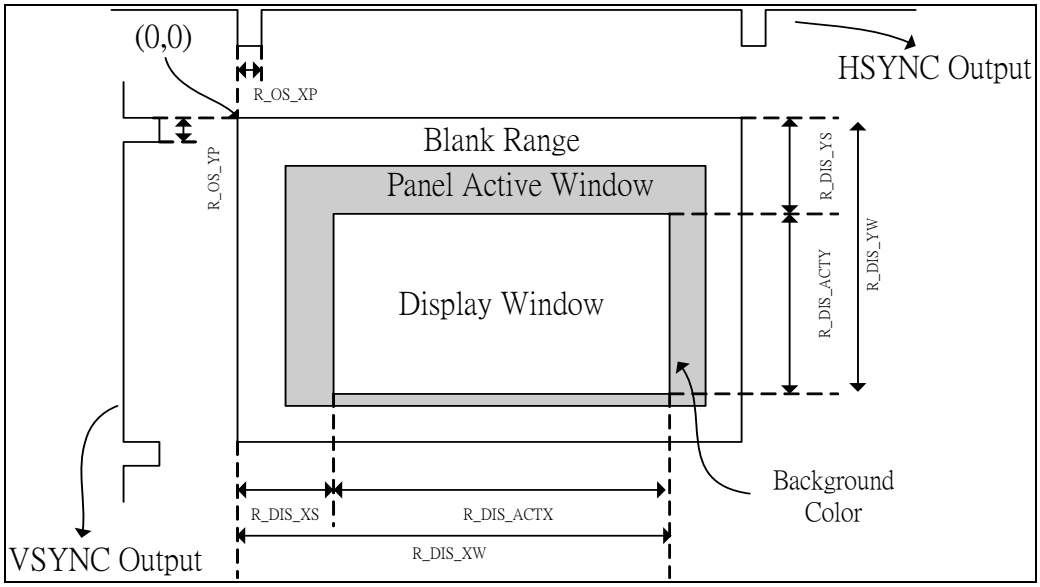


Figure 6-12 Display Window Setup

6.19 Scaling Engine

BIT1628A 可分別針對垂直(vertical)和水平(horizontal)方向做 Scaling 處理，其相關設定及說明如下：

6.19.1 Horizontal Scaling Down Engine

BIT1628A 可針對水平方向預作縮小處理，以符合 Buffer 深度。其相關設定請參考 **Table 6-20**。

Table 6-20 Horizontal Scale Down Register

Mnemonic	Address	R/W	Bits	Description	Default
R_PRESCX_START_S0	0x061[7:4], 0x05E[7:0]	RW	12	Horizontal Scaling Down Start Value for Switch2 Mode0	0x000
R_PRESCX_SHIFT_S0	0x061[2:0], 0x05F[7:0]	RW	11	Horizontal Scaling Down Shift Value for Switch2 Mode0	0x000
R_PRESCX_FIX_S0	0x062[5:4], 0x060[7:0]	RW	10	Horizontal Scaling Down Fix Value for Switch2 Mode0	0x000
R_PRESCX_EN_S0	0x062[0]	RW	1	Horizontal Scaling Down Enable for Switch2 Mode0 0: Disable (Bypass Mode) 1: Enable (Scale Mode)	0
R_PRESCX_FILTER_EN_S0	0x062[1]	RW	1	Horizontal Scaling Down Filter Enable for Switch2 Mode0 0: Disable (Bypass Mode) 1: Enable (Filter Mode)	0
R_PRESCX_FILTER_S0	0x062[2]	RW	1	Horizontal Scaling Down Filter Type for Switch2 Mode0 0: Bi-Linear Filter 1: Box Filter	0
R_PRE_FIX2_EN_S0	0x062[3]	RW	1	Scale down factor 2 enable for Switch2 Mode0 0: Disable (bypass Mode) 1: Enable (scale down 2 mode)	0
R_PRESCX_OVER_S0	0x062[7]	RW	1	Scale down factor over 2 for Switch2 Mode0 0: Disable (factor under 2)	0

				1: Enable (factor over 2)	
R_PRESCX_START_S1	0x066[7:4], 0x063[7:0]	RW	12	Horizontal Scaling Down Start Value for Switch2 Mode1	0x088
R_PRESCX_SHIFT_S1	0x066[2:0], 0x064[7:0]	RW	11	Horizontal Scaling Down Shift Value for Switch2 Mode1	0x106
R_PRESCX_FIX_S1	0x067[5:4], 0x065[7:0]	RW	10	Horizontal Scaling Down Fix Value for Switch2 Mode1	0x000
R_PRESCX_EN_S1	0x067[0]	RW	1	Horizontal Scaling Down Enable for Switch2 Mode1 0: Disable (Bypass Mode) 1: Enable (Scale Mode)	0
R_PRESCX_FILTER_EN_S1	0x067[1]	RW	1	Horizontal Scaling Down Filter Enable for Switch2 Mode1 0: Disable (Bypass Mode) 1: Enable (Filter Mode)	1
R_PRESCX_FILTER_S1	0x067[2]	RW	1	Horizontal Scaling Down Filter Type for Switch2 Mode1 0: Bi-Linear Filter 1: Box Filter	0
R_PRE_FIX2_EN_S1	0x067[3]	RW	1	Scale down factor 2 enable for Switch2 Mode1 0:Disable (bypass Mode) 1: Enable (scale down 2 mode)	0
R_PRESCX_OVER_S1	0x067[7]	RW	1	Scale down factor over 2 for Switch2 Mode1 0: Disable (factor under 2) 1: Enable (factor over 2)	0

6.19.2 Horizontal Scaling UP Engine

BIT1628A 可針對水平方向作放大處理，以符合 Panel 解析度。其相關設定請參考 **Table 6-21**。

Table 6-21 Horizontal Scale UP Register

Mnemonic	Address	R/W	Bits	Description	Default
R_SCX1_START_S0	0x06B[1:0], 0x068[7:0]	RW	10	Horizontal Start Value for Switch2 Mode0	0x06C
R_SCX1_SHIFT_S0	0x069[7:0]	RW	8	Horizontal Zone 1 Shift Value for Switch2 Mode0	0xD8
R_SCX1_FIX_S0	0x06B[4:2], 0x06A[7:0]	RW	11	Horizontal Zone 1 Fix Value for Switch2 Mode0	0x230
R_SCX_FILTER_SEL_S0	0x06B[6:5]	RW	2	Horizontal Scaling Filter Type for Switch2 Mode0 11: Bypass Filter 10: Box Filter 01: Bi-Linear Filter 00: Catrom Filter	00
R_SCX_EN_S0	0x06B[7]	RW	1	Horizontal Scaling Enable for Switch2 Mode0 0: Disable (Bypass Mode) 1: Enable (Scale Mode)	0
R_SCX1_START_S1	0x06F[1:0], 0x06C[7:0]	RW	10	Horizontal Start Value for Switch2 Mode1	0x06C
R_SCX1_SHIFT_S1	0x06D[7:0]	RW	8	Horizontal Zone 1 Shift Value for Switch2 Mode1	0xF1
R_SCX1_FIX_S1	0x06F[4:2], 0x06E[7:0]	RW	11	Horizontal Zone 1 Fix Value for Switch2 Mode1	0x330
R_SCX_FILTER_SEL_S1	0x06F[6:5]	RW	2	Horizontal Scaling Filter Type for Switch2 Mode1 11: Bypass Filter 10: Box Filter 01: Bi-Linear Filter 00: Catrom Filter	11
R_SCX_EN_S1	0x06F[7]	RW	1	Horizontal Scaling Enable for Switch2 Mode1 0: Disable (Bypass Mode) 1: Enable (Scale Mode)	0
R_SCX2_SHIFT	0x070[7:0]	RW	8	Horizontal Zone 2 Shift Value	0x00
R_SCX2_FIX	0x074[2:0], 0x071[7:0]	RW	11	Horizontal Zone 2 Fix Value	0x000
R_SCX1_INC	0x074[5:4], 0x072[7:0]	RW	10	Non-Linear Increase Value	0x000
R_SCX2_DEC	0x074[7:6], 0x073[7:0]	RW	10	Non-Linear Decrease Value	0x000
R_ANZOOM_TYPE	0x075[0]	RW	1	Wide Screen Type 0: 3-Zone Wide Screen 1: Non-Liner Wide Screen	0
R_ANZOOM_EN	0x075[1]	RW	1	Wide Screen Mode Enable 0: Disable 1: Enable	0

6.19.3 Vertical Scaling Engine

BIT1628A 可依據 Auto Switch Mode 所選擇的模式(Mode0/Mode1)，自動切換適合的參數，針對影像垂直方向分別做放大或縮小處理，以符合 panel 解析度。其相關設定請參考 **Table 6-22**。

Table 6-22 Vertical Scale-Down Register

Mnemonic	Address	R/W	Bits	Description	Default
R_SCYE_START_M0	0x07A[1:0], 0x076[7:0]	RW	10	Vertical Start Value for EVEN Field on Switch Mode 0	0x009
R_SCYO_START_M0	0x07A[3:2], 0x077[7:0]	RW	10	Vertical Start Value for ODD Field on Switch Mode 0	0x0E0
R_SCY_SHIFT_M0	0x07A[4], 0x078[7:0]	RW	9	Vertical Shift Value on Switch Mode 0	0x098
R_SCY_FIX_M0	0x07A[6:5], 0x079[7:0]	RW	10	Vertical Fix Value on Switch Mode 0	0x100
R_SCY_RESAMPLE_M0	0x07A[7]	RW	1	Vertical Resample Filter on Switch Mode 0 0: Disable 1: Enable	1
R_SCY_EN_M0	0x07B[0]	RW	1	Vertical Scaling Function Enable on Switch Mode 0 0: Disable (Bypass Mode) 1: Enable (Scale Mode)	1
R_SCY_FILTER_EN_M0	0x07B[1]	RW	1	Vertical Scaling Filter Enable 0: Disable 1: Enable	1
R_SCY_FILTER_M0	0x07B[2]	RW	1	Vertical Scaling Filter Type on Switch Mode 0 0: Bi-linear Filter 1: Box Filter	0
R_LINE_MIRROR_M0	0x07B[4]	RW	1	Line buffer Mirror Enable on Switch Mode 0 0: Disable 1: Enable	0
R_LINE_CUT_M0	0x07B[5]	RW	1	Vertical Pre-Scaling Down Enable on Auto Switch Mode 0 0: Disable 1: Enable	0
R_CUT_MODE_M0	0x07B[6]	RW	1	Vertical Pre-Scaling Down Mode on Auto Switch Mode 0 0: EVEN Line 1: ODD Line	0
R_CUT_AUTO_M0	0x07B[7]	RW	1	Vertical Pre-Scaling Change Mode on Auto Switch Mode 0 0: Manual (R_CUT_MODE) 1: Auto (EVEN/ODD)	0
R_SCYE_START_M1	0x080[1:0], 0x07C[7:0]	RW	10	Vertical Start Value for EVEN Field on Switch Mode 1	0x040
R_SCYO_START_M1	0x080[3:2], 0x07D[7:0]	RW	10	Vertical Start Value for ODD Field on Switch Mode 1	0x0C0
R_SCY_SHIFT_M1	0x080[4], 0x07E[7:0]	RW	9	Vertical Shift Value on Switch Mode 1	0x080
R_SCY_FIX_M1	0x080[6:5], 0x07F[7:0]	RW	10	Vertical Fix Value on Switch Mode 1	0x000
R_SCY_RESAMPLE_M1	0x080[7]	RW	1	Vertical Resample Filter on Switch Mode 1 0: Disable 1: Enable	0

R_SCY_EN_M1	0x081[0]	RW	1	Vertical Scaling Function Enable on Switch Mode 1 0: Disable (Bypass Mode) 1: Enable (Scale Mode)	1
R_SCY_FILTER_EN_M1	0x081[1]	RW	1	Vertical Scaling Filter Enable 0: Disable 1: Enable	1
R_SCY_FILTER_M1	0x081[2]	RW	1	Vertical Scaling Filter Enable on Switch Mode 1 0: Bi-linear Filter 1: Box Filter	0
R_LINE_MIRROR_M1	0x081[4]	RW	1	Line buffer Mirror Enable on Switch Mode 1 0: Disable 1: Enable	0
R_LINE_CUT_M1	0x081[5]	RW	1	Vertical Pre-Scaling Down Enable on Auto Switch Mode 1 0: Disable 1: Enable	0
R_CUT_MODE_M1	0x081[6]	RW	1	Vertical Pre-Scaling Down Mode on Auto Switch Mode 1 0: EVEN Line 1: ODD Line	0
R_CUT_AUTO_M1	0x081[7]	RW	1	Vertical Pre-Scaling Change Mode on Auto Switch Mode 1 0: Manual (R_CUT_MODE) 1: Auto (EVEN/ODD)	0

6.20 Timing Adjustment

BIT1628A Timing 調整原則

1. IVREF(t1)總長度與 OVREF(t2)相近且小於 OVREF(t2)(參考 **Figure 6-13**)。
2. 修正 Line Buffer 所產生的 Error (Overflow or Underflow)。

Table 6-23 Timing Adjust Register

Mnemonic	Address	R/W	Bits	Description	Default
R_MASTER_DLY_M0	0x082[7:0]	RW	8	Output VSYNC synchronize Delay time (Base on IHSYNC) on switch mode 0	0x14
R_DLYE_OCLK_M0	0x085[7:4], 0x083[7:0]	RW	12	Even Field Output VSYNC synchronize Delay time(Base on LCLK) on switch mode 0	0x000
R_DLYO_OCLK_M0	0x085[3:0], 0x084[7:0]	RW	12	Odd Field Output VSYNC synchronize Delay time(Base on LCLK) on switch mode 0	0x000
R_MASTER_DLY_M1	0x086[7:0]	RW	8	Output VSYNC synchronize Delay time (Base on IHSYNC) on switch mode 1	0x13
R_DLYE_OCLK_M1	0x089[7:4], 0x087[7:0]	RW	12	Even Field Output VSYNC synchronize Delay time(Base on LCLK) on switch mode 1	0x190
R_DLYO_OCLK_M1	0x089[3:0], 0x088[7:0]	RW	12	Odd Field Output VSYNC synchronize Delay time(Base on LCLK) on switch mode 1	0x190

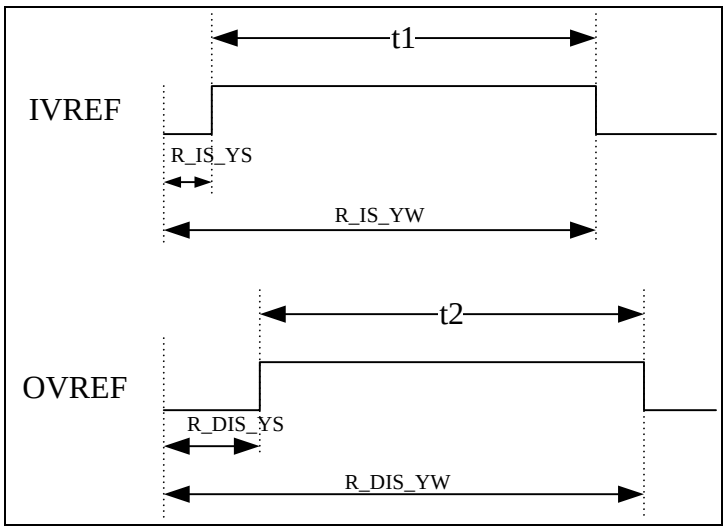


Figure 6-13 Timing Adjustment VREF Information

6.21 Image Enhancement

BIT1628A 提供多樣的調整機制，使用者可依據需求針對影像作調整，以獲得最佳之顯示效果。處理單元包括 Scaler 之前的前置處理與 Scaler 之後的後置處理兩部份。相關架構請參考下圖。

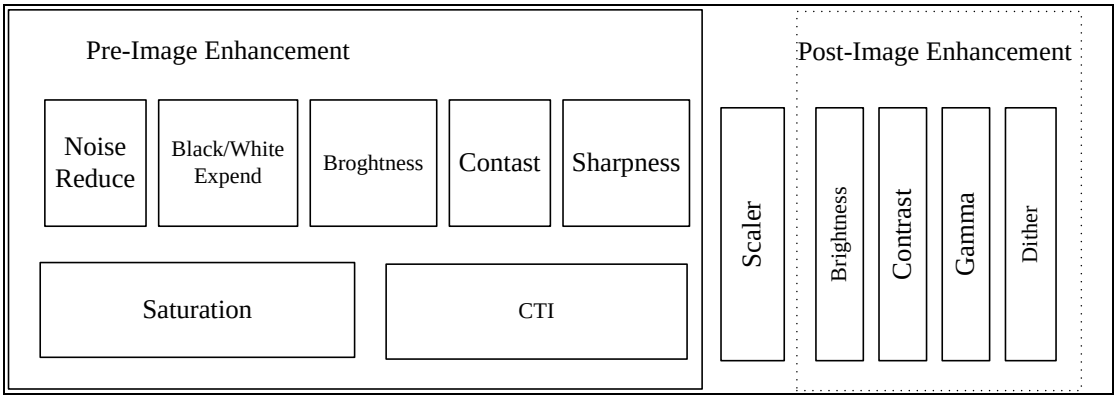


Figure 6-14 Image Enhancement

6.21.1 Post-Processing Brightness and Contrast

BIT1628A 針對 RGB Domain 的個別 Channel，分別提供 Brightness 和 Contrast 調整。其架構及相對應設定如下所示：

Table 6-24 Color Adjustment Register

Mnemonic	Address	R/W	Bits	Description	Default
R_BRIGHTNESS_R	0x08A[7:0]	RW	8	R Channel Brightness Value	0x80
R_BRIGHTNESS_G	0x08B[7:0]	RW	8	G Channel Brightness Value	0x80
R_BRIGHTNESS_B	0x08C[7:0]	RW	8	B Channel Brightness Value	0x80
R_CONTRAST_R	0x08D[7:0]	RW	8	R Channel Contrast Value	0x80
R_CONTRAST_G	0x08E[7:0]	RW	8	G Channel Contrast Value	0x80
R_CONTRAST_B	0x08F[7:0]	RW	8	B Channel Contrast Value	0x80
R_CONTRAST_RGB_MODE	0x092[0]	RW	1	Post-Contrast Adjust Type 0: Type 1 1: Type 2	0

6.21.2 Dither

BIT1628A 內建 User Programmable Dither Function 能使 6 Bits Panel Display 得到更佳的顯示品質，相關 Register 請參考下表。

Table 6-25 Dither Register					
Mnemonic	Address	R/W	Bits	Description	Default
R_DITHER_L0	0x090[7:0]	RW	8	Line 0 Dither Factor	0x39
R_DITHER_L1	0x091[7:0]	RW	8	Line 1 Dither Factor	0x53
R_DITHER_EN	0x092[2]	RW	1	Dither Function Enable 0: Disable 1: Enable	1

6.21.3 LUT Gamma Correction

BIT1628A 內建 LUT-base Gamma Correction Function，其相關記憶體對應爲 0x200~0x2FF 及 Register 請參考 **Table 6-26**。

Table 6-26 LUT Gamma Register					
Mnemonic	Address	R/W	Bits	Description	Default
R_GAMMA_ EN	0x092[7]	RW	1	GAMMA LUT Enable 0: Gamma RAM R/W mode 1: Gamma Correction mode	0
R_GAMMA_SEL	0x092[5:4]	RW	2	GAMMA LUT RAM R/W Select 00: Red 01: Green 10: Blue 11: Write RGB, Read Forbiddance	00

6.21.4Pre-Processing Brightness/Contrast Adjustment

BIT1628A 針對 Y Domain 提供 Blacklevel 、Brightness 和 Contrast 的調整。相對應設定如下所示：

Table 6-27 Pre-Processing Brightness / Contrast Register					
Mnemonic	Address	R/W	Bits	Description	Default
R_BLACKLEVEL	0x093[7:0]	RW	8	Black-Level Value Adjustment range (-128 ~ +127) 0x00=-128, 0x80=0, 0xFF=+127	0x80
R_BRIGHTNESS	0x094[7:0]	RW	8	Brightness Value Adjustment range (-128 ~ +127) 0x00=-128, 0x80=0, 0xFF=+127	0x80
R_CONTRAST	0x095[7:0]	RW	8	Contrast Value Adjustment range (0.0 ~ 1.9922) 0x00=0.0, 0x80 = 1, 0xFF=1.9922	0x80

6.21.5Black and White expand Adjustment

BIT1628A 針對 Y Domain 提供 Black and White Expand 的調整。可以針對影像中的黑與白的部份延展使得可以表現出更多的階數，相對應設定如下所示：

Table 6-28 Black and White expand Register					
Mnemonic	Address	R/W	Bits	Description	Default
R_EXPAND_EN	0x096[7]	RW	1	Black and White Expand Enable 0: Disable 1: Enable	0
R_BLACK_START	0x096[6:0]	RW	7	Black Zone End point	0x7F
R_WHITE_START	0x097[7:0]	RW	8	White Zone Start point	0x00
R_NORMAL_SLOPE	0x099[7:0]	RW	8	Contrast Value for Middle zone Adjustment range (0.0 ~ 1.9922) 0x00=0.0, 0x80 = 1, 0xFF=1.9922	0x80
R_BLACK_SLOPE	0x098[7:0]	RW	8	Contrast Value for Black zone Adjustment range (0.0 ~ 1.9922) 0x00=0.0, 0x80 = 1, 0xFF=1.9922	0x80
R_WHITE_SLOPE	0x09A[7:0]	RW	8	Contrast Value for White zone Adjustment range (0.0 ~ 1.9922) 0x00=0.0, 0x80 = 1, 0xFF=1.9922	0x80

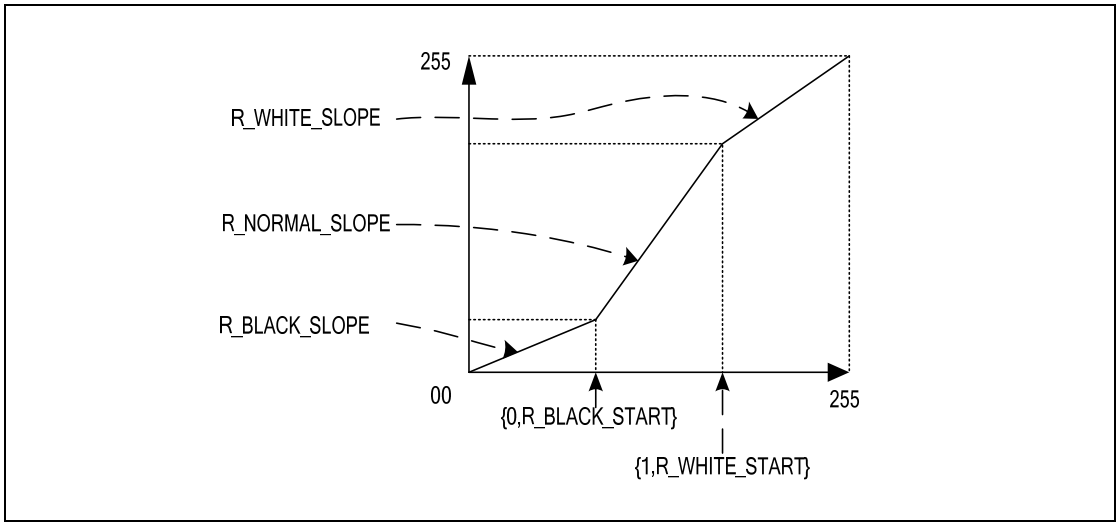


Figure 6-15 Image Enhancement

6.21.6 Sharpness Process

BIT1628A 針對 Y Domain Data 提供 sharpness 處理可強化影像之銳利度，其相對應設定如下所示：

Table 6-29 Sharpness and Smoothness Process Register

Mnemonic	Address	R/W	Bits	Description	Default
R_UNSHARP_VAL	0x09B[6:0]	RW	7	Sharpness value (0~127) 0x00: Least sharpness 0x7F: Most sharpness	0x7F
R_UNSHARP_EN	0x09B[7]	RW	1	Sharpness Enable 0: Disable 1: Enable	1
R_UNSHARP_THD	0x09C[5:0]	RW	6	Sharpness Threshold Value	0x00
R_UNSHARP_TYPE	0x09C[6]	RW	1	Sharpness Filter Type 0: Type 1 1: Type 2	1

6.21.7 Saturation and Kill Color Process

BIT1628A 針對 UV Domain Data 提供 Saturation 和 Kill Color 的處理，其相對應設定如下所示：

Table 6-30 UV Domain Register

Mnemonic	Address	R/W	Bits	Description	Default
R_SAT_U	0x09D[7:0]	RW	8	U Saturation Value Adjustment range (0.0 ~ 3.98) 0x00=0.0, 0x40=1.0, 0xFF=3.98	0x55
R_SAT_V	0x09E[7:0]	RW	8	V Saturation Value Adjustment range (0.0 ~ 3.98) 0x00=0.0, 0x40=1.0, 0xFF=1.9843	0x55
R_SAT_MODE	0x09F[0]	RW	1	V Saturation Value reference with R_SAT_U 0: Disable 1: Simultaneously adjust R_SAT_U and R_SAT_V (From R_SAT_U)	0
R_KILL_COLOR	0x09F[1]	RW	1	Control Kill Color enable 0: Disable 1: Enable	0
R_KILL_COLOR_THD	0x09F[6:2]	RW	5	Auto Kill Color when below Threshold Value	0

6.21.8 Chroma Transient Improvement (CTI)

BIT1628A 提供 Chroma Transient Improvement (CTI)，相關 Register 請參考 **Table 6-31**

Table 6-31 Chroma Transient Improvement Register

Mnemonic	Address	R/W	Bits	Description	Default
R_CTI_GA	0x0A0[1:0]	RW	2	CTI Gain Value	00
R_CTI_LI	0x0A0[3:2]	RW	2	CTI Limit Value	10
R_CTI_NEW	0x0A0[4]	RW	1	CTI Factor1 Select 0: Type 1 1: Type 2	0
R_CTI_NEW2	0x0A0[5]	RW	1	CTI Factor2 Select 0: Type 1 1: Type 2	0
R_CTI_CMO	0x0A0[6]	RW	1	CTI CMO Mode Enable 0: Disable 1: Enable	0
R_CTI_EN	0x0A0[7]	RW	1	CTI Enable 0: Disable 1: Enable	1
R_CTI_CMO_VAL	0x0A1[3:0]	RW	4	CTI CMO Mode Threshold Value	0x4
R_CTI_USEL	0xA1[4]	RW	1	CTI Process refer U Channel 0: Disable 1: Enable	1
R_CTI_VSEL	0xA1[5]	RW	1	CTI Process refer V Channel 0: Disable 1: Enable	1

6.21.9Noise Reduce Filter

BIT1628A 提供 Noise Reduce Filter 處理，可針對影像中雜點先做濾除，其相對應設定如下所示：

Table 6-32 Noise reduce Filter Register

Mnemonic	Address	R/W	Bits	Description	Default
R_NR_YTHD	0x0A3[4:0]	RW	5	Noise Reduce Filter Threshold Value for Y Domain	0x10
R_NR_YSEL	0x0A3[6:5]	RW	2	Noise Reduce Filter Select for Y Domain	00
R_NR_YEN	0x0A3[7]	RW	1	Noise Reduce Filter Enable for Y Domain 0: Disable 1: Enable	0
R_NR_UVTHD	0x0A4[4:0]	RW	5	Noise Reduce Filter Threshold Value for UV Domain	0x00
R_NR_UVSEL	0x0A4[6:5]	RW	2	Noise Reduce Filter Select for UV Domain	00
R_NR_UVEN	0x0A4[7]	RW	1	Noise Reduce Filter Enable for UV Domain 0: Disable 1: Enable	0
R_NR_UVTHD_MAX	0x0A5[7:2]	RW	6	Noise Reduce Max Threshold Value for UV Domain	0x18

6.21.10 Double Buffer

BIT1628A 在 Image Enhance adjustment 提供 Double Buffer Register，提供給使用者針對這些 Register 可以做 Parallel update，其相關架構請參考，相關設定 Register 請參考。

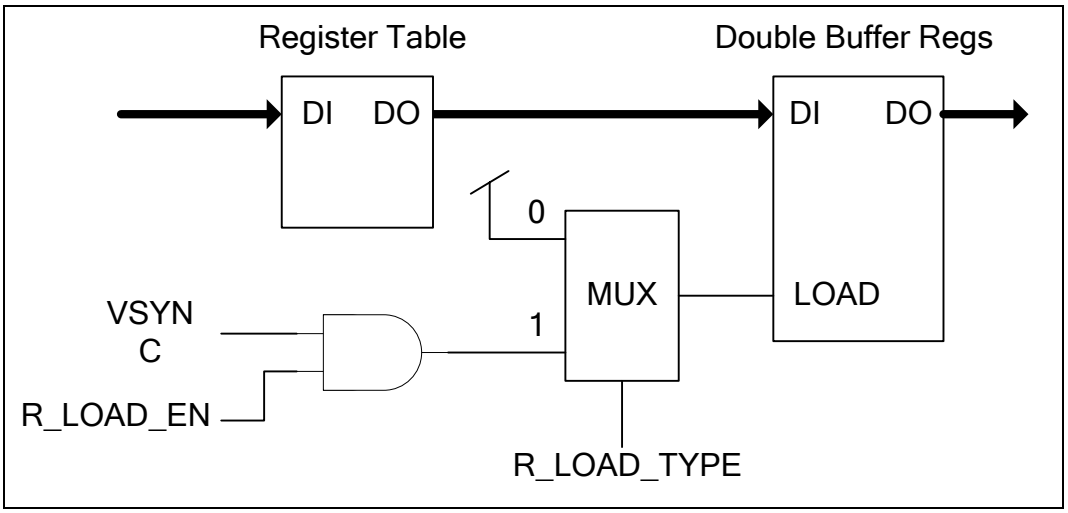


Figure 6-16 Double Buffer Function

Table 6-33 Double Buffer Register

Mnemonic	Address	R/W	Bits	Description	Default
R_LOAD_EN	0x0A5[7]	RW	1	Double Buffer Load Enable 0: Nothing 1: Load	0
R_LOAD_TYPE	0x0A5[6]	RW	1	Double Buffer Register Update Type 0: Immediately 1: Control by R_LOAD_EN	0

6.22 Video Decoder

6.22.1 Video Decoder Feature

- One 10-bit video CMOS Analog-to-Digital Converters (ADCs) in differential CMOS style for best S/N-performance
- Fully programmable static gain or automatic gain control (AGC) for the selected CVBS or Y/C channel : 0~12db (Analog) and 0~18db (Digital)
- Automatic Clamp Control (ACC) for CVBS, Y and C
- On-chip clock generator
- Digital PLL for synchronization and clock generation from all standards and non-standard video sources e.g. consumer grade VTR
- Requires only one crystal for all standards (crystal value could adjust)
- Automatic detection of 50 and 60 Hz field frequency, and automatic switching between PAL and NTSC standards
- Accepts NTSC (J, M, 4.43), PAL (60, B, D, G, H, I, M, N), and SECAM (B, D, G, K, K1, L) video signal
- User programmable luminance peaking or aperture correction
- Adaptive 3/5-line comb filter for two dimensional chrominance/luminance separation
- PAL delay line for correcting PAL phase errors
- Hue control on-chip
- Multi-standard VBI-data slicer decoding closed caption
- MV copy protection detection

6.22.2 Video Decoder Architectures

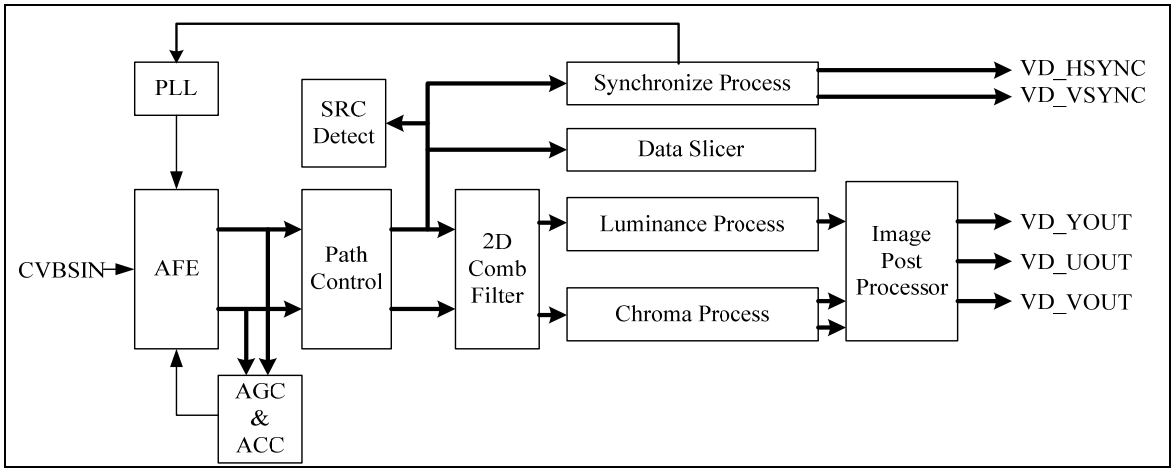


Figure 6-17 Video Decoder Block Diagram

6.22.3Comb Filter Process

BIT1628A Video Decoder 提供 NTSC 3-Line 和 PAL 5-Line 的 Adaptive Comb Filter 來做 Y/C 分離，其相關設定請參考下表。

Table 6-34 Comb filter process Register

Mnemonic	Address	R/W	Bits	Description	Default
R_COMBY_EN	0x0A6[7:0]	RW	8	COMB Y Enable	0xFF
R_COMBC_EN	0x0A7[7:0]	RW	8	COMB C Enable [0]: PAL/PAL-60 [1]: PAL_N [2]: SECAM [3]: PAL_M [4]: NTSC_4.43_50Hz [5]: NTSC_M / NTSC_J [6]: NTSC_4.43_60Hz [7]: Black & White	0XFF
R_COMBY_VAL	0x0A8[3:0]	RW	4	COMB Y factor	0xF
R_COMBC_VAL	0x0A8[7:4]	RW	4	COMB C factor	0xF
R_COMB_PSEL	0x0A9[0]	RW	1	COMB Phase Select 0: Manual(refer R_COMB_PHASE) 1: Auto	0
R_COMB_PHASE	0x0A9[1]	RW	1	COMB Phase Select 0: 0-90-180-270-0 1: 0-180-0	1
R_COMB_VTRC	0x0A9[2]	RW	1	COMB VTRC Mode enable 0: Disable 1: Enable	1
R_COMBY_SEL	0x0A9[7:5]	RW	3	COMB Y factor	000

6.22.4Luminance Process

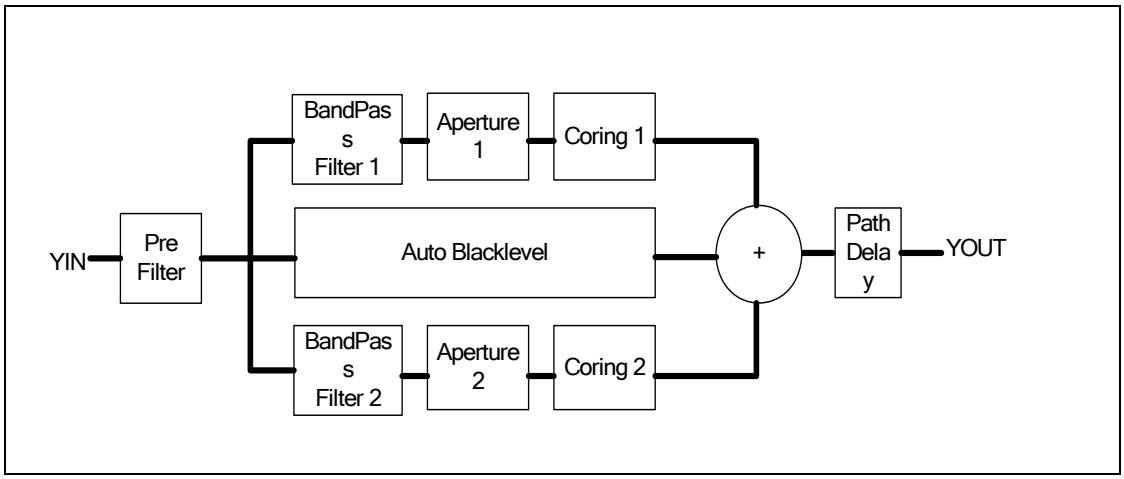


Figure 6-18 Luminance process block

Table 6-35 Luminance Process Register					
Mnemonic	Address	R/W	Bits	Description	Default
R_VD_BLACKLEVEL	0x0AA[7:0]	RW	8	Black Level Value	0x00
R_BPASS_SEL1	0x0AB[1:0]	RW	2	Band Pass 1 Frequency Select 00: Frequency 1 01: Frequency 2 10: Frequency 3 11: Frequency 4	00
R_COR_SEL1	0x0AB[3:2]	RW	2	Coring 1 circuit amplitude value 00: Coring factor 1 01: Coring factor 2 10: Coring factor 3 11: Coring factor 4	00
R_APER_SEL1	0x0AB[5:4]	RW	2	Aperture 1 Factor 00: 0 01: 0.25 10: 0.5 11: 1.0	00
R_APER_TYPE1	0x0AB[6]	RW	1	Aperture 1 Type 0: Minus 1: Plus	0
R_APER_EN1	0x0AB[7]	RW	1	Aperture 1 Enable 0: Disable 1: Enable	1
R_BPASS_SEL2	0x0AC[1:0]	RW	2	Band Pass 2 Frequency Select 00: Frequency 1 01: Frequency 2 10: Frequency 3 11: Frequency 4	00
R_COR_SEL2	0x0AC[3:2]	RW	2	Coring 2 circuit amplitude value 00: Coring factor 1 01: Coring factor 2 10: Coring factor 3 11: Coring factor 4	00
R_APER_SEL2	0x0AC[5:4]	RW	2	Aperture 2 Factor 00: 0 01: 0.25 10: 0.5	00

				11: 1.0	
R_APER_TYPE2	0x0AC[6]	RW	1	Aperture 2 Type 0: Minus 1: Plus	0
R_APER_EN2	0x0AC[7]	RW	1	Aperture 2 Enable 0: Disable 1: Enable	1
R_YDEL	0x0AD[3:0]	RW	4	Y Data Path Delay 1111: Delay 16 Clocks 1000: Delay 0 Clock 0000: Delay -15 Clocks	0x8
R_LUMA_DITHER	0x0AD[5:4]	RW	2	Y Dither Process 00: Disable Dither 01: 8 Bits Dither 10: 7 Bits Dither 11: 6 Bits Dither	00
R_PREF_EN	0x0AD[7]	RW	1	Luma Pre-Filter Enable 0: Disable 1: Enable	0
R_LUMA_COMP_AUTO	0x0AE[0]	RW	1	Auto Black Level Compensate 0: Disable (refer R_LUMA_COMP) 1: Enable	1
R_LUMA_COMP	0x0AE[1]	RW	1	Black Level Compensate enable 0: Disable 1: Enable	0
R_BLACKLEVEL_UPDATE	0x0AE[4]	RW	1	Black Level update enable 0: Disable (keep old value) 1:Enable	0
R_BLACKLEVEL_AUTO	0x0AE[5]	RW	1	Auto Black Level tracker 0: Disable 1: Enable	1

6.22.5Synchronization Process

Synchronization Process Block 從 Y/C 分離後的 Luminance 的信號中，分離解出 HSYNC 和 VSYNC 的信號。

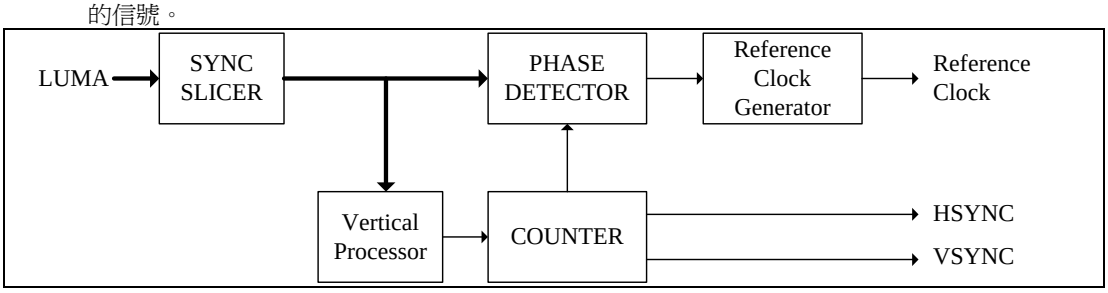


Figure 6-19 Synchronization Process

Table 6-36 Synchronization process Register					
Mnemonic	Address	R/W	bit	Description	Default
R_SYNC_IDEL	0x0AF[7:0]	RW	8	Horizontal increment delay	0x97
R_SYNC_HSYS	0x0B0[7:0]	RW	8	Horizontal Sync Start	0x00
R_SYNC_HCS	0x0B1[7:0]	RW	8	Clamp Signal Start	0x00
R_SYNC_HSS	0x0B2[7:0]	RW	8	Horizontal Delay	0xFF
R_BGPU_POINT_N	0x0B3[5:0]	RW	6	Burst Start point for 60Hz Signal	0x0D
R_BGPU_POINT_P	0x0B4[5:0]	RW	6	Burst Start point for 50Hz Signal	0x0D
R_SLICER_THD	0x0B5[7:0]	RW	8	Sync-Slicer Threshold	0x00
R_VNOISE_MODE	0x0B6[1:0]	RW	2	Vsync Noise Reduction Mode 00: Normal Mode 01: Fast Mode 10: Free-run Mode 11: Bypass Mode	00
R_VTRC	0x0B6[2]	RW	1	VCR Mode Enable 0: Disable 1: Enable	0
R_AUTO_VTRC	0x0B6[3]	RW	1	Auto VCR Mode 0: Disable 1: Enable	1
R_FIDT_THD	0x0B6[7:4]	RW	4	50/60Hz Detection Threshold	0x8
R_SYNC_LPADJ	0x0B7[1:0]	RW	2	Loop filter tracker speed	00
R_SYNC_PDGAIN	0x0B7[3:2]	RW	2	Loop filter Phase tracker factor	00
R_SYNC_LPLMT	0x0B7[4]	RW	1	Loop filter Phase adjustment speed	1
R_SYNC_HPLL	0x0B7[6:5]	RW	2	PLL Free-run Mode Enable 00: Free-run on 23.928MHz 01: Disable (Normal) 10: Free-run on 27MHz 11: Free-run on 30.07MHz	01
R_SYNC_CHT_EN	0x0B7[7]	RW	1	Chroma Tarp Filter enable 0: Disable 1: enable	1
R_DTO_REF	{0x0BA[1:0],0x0B9[7:0],0x0B8[7:0]}	RW	18	DTO reference frequency	0x11940
R_SYNC_DLY	0x0BA[7]	RW	1	Comb line buffer timing Delay 0: Disable 1: Enable	1
R_SYNC_CDEL	{0x0BA[6],0x0BB[7:0]}	RW	9	Horizontal increment delay for chroma	0x97

6.22.6 Chroma Process

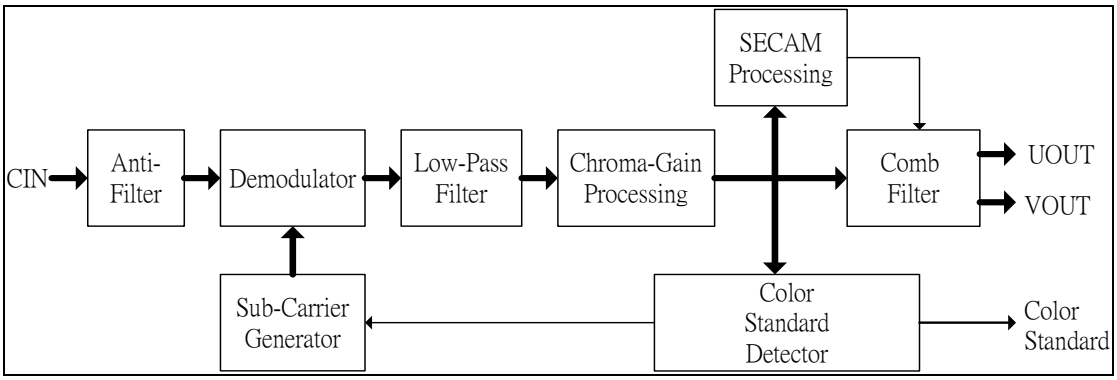


Figure 6-20 Chroma Process Function Block

Table 6-37 Chroma Process Register					
Mnemonic	Address	R/W	Bits	Description	Default
R_CHROMA_CNT	{0x0BC[2:0],0x0BD[7:0]}	RW	11	Chroma shift count	000
R_STD_SECAM_EN	0x0BC[3]	RW	1	SECAM Standard Enable	1
R_STD_PALM_EN	0x0BC[4]	RW	1	PAL-M Standard Enable	1
R_STD_PALN_EN	0x0BC[5]	RW	1	PAL-N Standard Enable	1
R_STD_NTSC4_60_EN	0x0BC[6]	RW	1	NTSC4.43MHz 60Hz Standard Enable	1
R_STD_NTSC4_50_EN	0x0BC[7]	RW	1	NTSC4.43MHz 50Hz Standard Enable 0: Disable 1: Enable	1
R_CHROMA_GAIN	0x0BE[6:0]	RW	7	Chroma Fixed-Gain Value 000000: Minimum gain (0.25) 010000: Normal gain (1.0) 111111: Maximum gain (3.5)	0x20
R_CHROMA_GAIN_SEL	0x0BE[7]	RW	1	Chroma Gain Type Select 0: Auto-Gain 1: Fixed-Gain (Defined on 0x609[6:0])	0
R_GAIN_CTL_VALUE	0x0C1[1:0],0x0BF[7:0]	RW	10	Chroma Gain Reference value	0x1C0
R_GAIN_SECAM_VALUE	0x0C1[3:2],0x0C0[7:0]	RW	10	SECAM Chroma Gain Reference Value	0x152
R_GAIN_CTRL_SPEED	0x0C1[5:4]	RW	2	Auto Chroma Gain Loop Filter 00: Slow time constant 01: Medium time constant 10: Fast time constant 11: Frozen	10
R_SCXR	0x0C1[7]	RW	1	SECAM Cross Color Reduction 0: Disable 1: Enable	0
R_THRESHOLD_SECAM	0x0C2[7:0]	RW	8	Color Killer Threshold for SECAM	0xFF
R_THRESHOLD_QAM	0x0C3[7:0]	RW	8	Color Killer Threshold for PAL and NTSC	0x80
R_SECAM_SENSITIVE	0x0C4[7:0]	RW	8	SECAM switch sensitive level	0x40
R_PAL_SENSITIVE	0x0C5[7:0]	RW	8	PAL switch sensitive level	0x50
R_STD_OFF00	0x0C6[7:0]	RW	8	Burst Freq. offset for 3.57MHz	0x00
R_STD_OFF01	0x0C7[7:0]	RW	8	Burst Freq. offset for 4.2MHz	0x00
R_STD_OFF10	0x0C8[7:0]	RW	8	Burst Freq. offset for 4.43MHz	0x00
R_CHROMA_HUE	0x0C9[7:0]	RW	8	Chroma HUE Value	0x00
R_CHROMA_LPPI1	0x0CA[1:0]	RW	2	Chroma Low Pass Filter Factor 1	01
R_CHROMA_LPPI2	0x0CA[3:2]	RW	2	Chroma Low Pass Filter Factor 2	11
R_SQP_LMT	0x0CA [4]	RW	1	Sub-Carrier Frequency Select 0: Type 1	0

				1: Type 2	
R_SQP_LPPI	0x0CA[6:5]	RW	2	Sub-Carrier Phase Detection factor 1	01
R_SQP_SPUP	0x0CA[7]	RW	1	Sub-Carrier Phase Detection factor 2	0
R_COMPENSATE_SEL	0x0CB[0]	RW	1	Burst tracker Mode 0: Frequency Mode 1: Phase Mode	1
R_STD_CKILL	0x0CB[1]	RW	1	Auto Color Kill From Color Detection 0: Disable 1: Enable(Auto kill from color detection)	1
R_CHROMA_PHASE	0x0CB[2]	RW	1	Chroma Phase Detection Mode 0: Mode 1 1: Mode 2	0
R_SECAM_GAINDIS	0x0CB[3]	RW	1	SECAM Gain Disable tracker 0: Disable 1: Enable	1
R_CDV_SEL	0x0CB[4]	RW	1	TV / VCR Mode Select 0: Mode 1 1: Mode 2	0
R_CHROMA_RCF_EN	0x0CB[5]	RW	1	Re-Comb Filter Enable 0: Disable 1: Enable	1

6.22.7 AGC and ACC Process

BIT1628A 提供 AGC (Auto Gain Control)功能以控制 Analog PGA 所提供 -6db、 0db、 6db 和 12db 四種的 Gain value 及 Digital PGA 所提供+18db ~ -18db Linear Digital PGA，及提供 ACC (Auto Clamp Control)功能以控制 Analog Clamp 和 Digital Clamp。AGC 及 ACC 的控制可使輸入信號維持在正常的振幅及準位，使得輸出的結果不會隨著信號的漂移改變而有所變化，進而影響畫面的穩定度。相關的示意圖請參考下圖，相關的 Register 設定請參考下表。

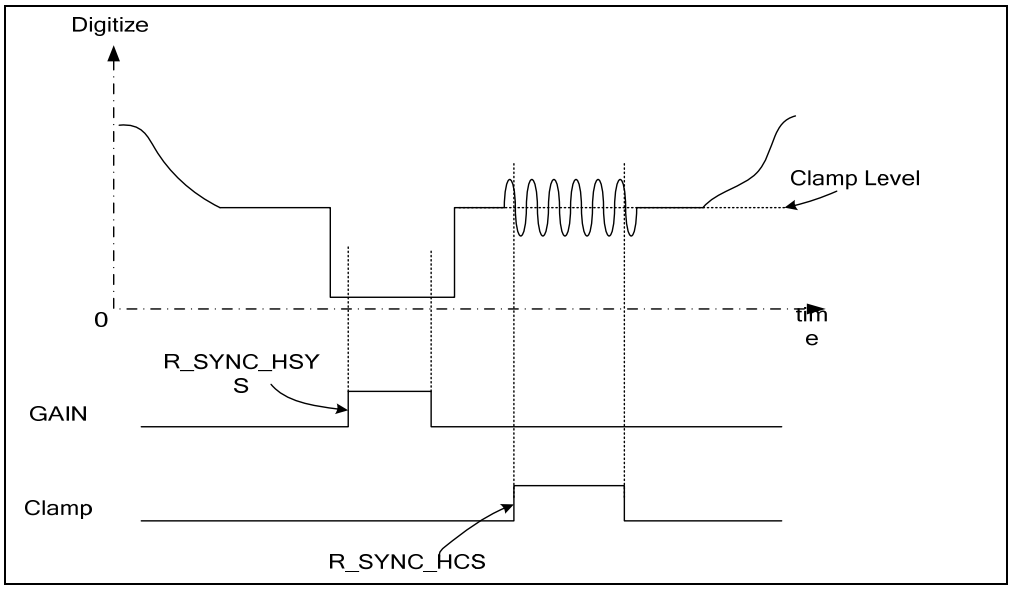


Figure 6-21 AGC and Clamp pulse

Table 6-38 AGC Control Register

Mnemonic	Address	R/W	Bits	Description	Default
R_ACLAMP_SPEED_M	0x0CC[7:6]	RW	2	Analog Clamp Tracker Speed Mode 00: Manual Mode refer R_ACLAMP_SPEED 01: Auto Slow Mode	

				10: Auto medium Mode	
				11: Auto Fast Mode	
R_ACLAMP1_LEVEL	0x0CE[7:0]	RW	8	Analog Clamp 1 Level	0x80
R_ACLAMP1_THD	0x0CF[1:0]	RW	2	Analog Clamp 1 Threshold	01
R_UPDN11_SEL	0x0CF[2]	RW	1	Channel AIN11 Clamp select 0: Aclamp1 1: Aclamp2	1
R_UPDN12_SEL	0x0CF[3]	RW	1	Channel AIN12 Clamp select 0: Aclamp1 1: Aclamp2	0
R_ACLAMP1_EN	0x0CF[7]	RW	1	Analog Clamp 1 Enable 0: Disable (turn off Analog Clamp) 1: Enable	1
R_ACLAMP2_LEVEL	0x0D0[7:0]	RW	8	Analog Clamp 2 Level	0x44
R_ACLAMP2_THD	0x0D1[1:0]	RW	2	Analog Clamp 2 Threshold	01
R_UPDN2_SEL	0x0D1[2]	RW	1	Channel AIN2 Clamp select 0: Aclamp1 1: Aclamp2	1
R_ACLAMP2_EN	0x0D1[7]	RW	1	Analog Clamp 2 Enable 0: Disable (turn off Analog Clamp) 1: Enable	1
R_AGC_UPPER	0x0D2[7:0]	RW	8	Analog Gain tracker High limit	0x35
R_AGC_LOWER	0x0D3[7:0]	RW	8	Analog Gain tracker Low limit	0x2B
R_AAGC_VALUE	0x0D4[1:0]	RW	2	Analog Gain tracker start value 00: -6 db (x0.5) 01: 0 db (x1) 10: 6 db (x2) 11: 12 db (x4)	10
R_AGC1_SEL	0x0D4[2]	RW	1	Analog GAIN 1 select 0: From Fixed Gain 1: From Auto tracker Gain	0
R_AGC2_SEL	0x0D4[3]	RW	1	Analog GAIN 2 select 0: From Fixed Gain 1: From Auto tracker Gain	1
R_AAGC_HOLD	0x0D4[6]	RW	1	Analog Gain tracker Hold 0: Disable 1: Enable	0
R_AAGC_EN	0x0D4[7]	RW	1	Analog Gain tracker Enable 0: Disable 1: Enable	1
R_GAIN1_VAL[1:0]	0x0D5[1:0]	RW	2	Analog Fixed Gain 1 Value	01
R_GAIN1_SEL	0x0D5[3]	RW	1	Analog Gain 1 Select 0: Fixed Gain (refer R_GAIN1_VAL) 1: Auto Gain (refer auto tracker gain value)	0
R_GAIN2_VAL[1:0]	0x0D5[5:4]	RW	2	Analog Fixed Gain 2 Value	01
R_GAIN2_SEL	0x0D5[7]	RW	1	Analog Gain 2 Select 0: Fixed Gain (refer R_GAIN2_VAL) 1: Auto Gain (refer auto tracker gain value)	0
R_DCLAMP11_LEVEL	0x0D7[1:0],0x0D6[7:0]	RW	10	Digital Clamp 11 Level	0x19A
R_DCLAMP11_THD	0x0D7[3:2]	RW	2	Digital Clamp 11 Threshold	01
R_DCLAMP11_SEL	0x0D7[4]	RW	1	Digital Clamp 11 Value Select 0: from Digital Clamp 11 tracker value 1: from Digital Clamp 2 tracker value	1
R_DCLAMP11_HOLD	0x0D7[6]	RW	1	Digital Clamp 11 tracker Hold	0

				0: Disable	
				1: Enable	
R_DLCMPA11_EN	0x0D7[7]	RW	1	Digital Clamp 11 Enable	1
				0: Disable	
				1: Enable (auto tracker)	
R_DCLAMP12_LEVEL	0x0D9[1:0],0x0D8[7:0]	RW	10	Digital Clamp 12 Level	0x19A
R_DCLAMP12_THD	0x0D9[3:2]	RW	2	Digital Clamp 12 Threshold	01
R_DCLAMP12_SEL	0x0D9[4]	RW	1	Digital Clamp 12 Value Select	1
				0: from Digital Clamp 12 tracker value	
				1: from Digital Clamp 2 tracker value	
R_DCLAMP12_HOLD	0x0D9[6]	RW	1	Digital Clamp 12 tracer Hold	0
				0: Disable	
				1: Enable	
R_DLCMPA12_EN	0x0D9[7]	RW	1	Digital Clamp 12 Enable	1
				0: Disable	
				1: Enable (auto tracker)	
R_DCLAMP2_LEVEL	0x0DB[1:0],0x0DA[7:0]	RW	10	Digital Clamp 2 Level	0x070
R_DCLAMP2_THD	0x0DB[3:2]	RW	2	Digital Clamp 2 Threshold	01
R_DCLAMP_STABLE_VS	0x0DB[4]	RW	1	Stable control VSYNC Mode for Digital Clamp	1
				0: Disable	
				1: Enable	
R_DCLAMP_STABLE_EN	0x0DB[5]	RW	1	Stable control for Digital Clamp	1
				0: Disable	
				1: Enable	
R_DCLAMP2_HOLD	0x0DB[6]	RW	1	Digital Clamp 2 tracer Hold	0
				0: Disable	
				1: Enable	
R_DCLAMP2_EN	0x0DB[7]	RW	1	Digital Clamp 2 Enable	1
				0: Disable	
				1: Enable (auto tracer)	
R_DCLAMP2_DIFF_THD	0x0DC[7:0]	RW	8	Digital Clamp Stable Mode difference threshold	
R_DGAIN1_VAL	0x0DF[1:0],0x0DD[7:0]	RW	10	Digital Gain 1 Fixed Value	0x000
R_DGAIN1_SEL	0x0DF[3]	RW	1	Digital Gain 1 Select	0
				0: Fixed gain (refer R_DGAIN1_VAL)	
				1: Auto gain	
R_DGAIN2_VAL	0x0DF[5:4],0x0DE[7:0]	RW	10	Digital Gain 2 Fixed Value	0x000
R_DGAIN2_SEL	0x0DF[7]	RW	1	Digital Gain 2 Select	0
				0: Fixed gain (refer R_DGAIN2_VAL)	
				1: Auto gain	
R_DAGC_LEVEL	0x0E1[1:0],0xE0[7:0]	RW	10	Digital Gain Tracer Level	0x06E
R_DAGC_SPEED	0xE1[3:2]	RW	2	Digital Gain Tracer Speed	1
				00: Fixed 1	
				01: Fixed 2	
				10: Auto Slow Mode	
				11: Auto Fast Mode	
R_DAGC_STABLE_VS	0x0E1[4]	RW	1	Stable control VSYNC Mode for Digital Gain	0
				0: Disable	
				1: Enable	
R_DAGC_STABLE_EN	0x0E1[5]	RW	1	Stable control for Digital Gain	1
				0: Disable	
				1: Enable	
R_DAGC_HOLD	0x0E1[6]	RW	1	Digital Gain Tracer Hold	0
				0: Disable	
				1: Enable	
R_DAGC_EN	0x0E1[7]	RW	1	Digital Gain Tracer Enable	1

				0: Disable 1: Enable	
R_DAGC_DIFF_THD	0x0E2[3:0]	RW	4	Digital Gain Stable Mode difference threshold	0100
R_N_OVER1	0x0CD[3:0]	RW	4	Overflow detect Threshold1 For NTSC	0000
R_N_OVER2	0x0CD[7:4]	RW	4	Overflow detect Threshold2 For NTSC	0000
R_P_OVER1	0x0E3[3:0]	RW	4	Overflow detect Threshold1 For PAL	0000
R_P_OVER2	0x0E3[7:4]	RW	4	Overflow detect Threshold2 For PAL	0000
R_OVER_SEL	0x0E2[6]	RW	1	Overflow detect Threshold Select 0: refer R_N_OVER1 and R_N_OVER2 1: refer R_P_OVER1 and R_P_OVER2	0
R_OVER_AUTO	0x0E2[7]	RW	1	Overflow detect Threshold mode 0: Manual refer R_OVER_SEL setting 1: Auto Mode	1
R_ADC_RAW	0x0E8[6]	RW	1	Reference analog Source select 0: ADC1 1: ADC2	1

6.22.8 VBI Data Slicer

BIT1628A 提供 Data Slicer 功能可依據針對所設定的 Lines 及 Even/Odd，分離出 16 Bits 的 data，並且經由 Interrupt 及 Register 提供 MCU 做後續處理，相關的 Register 請參考下表。

Table 6-39 VBI data slicer Process Register

Mnemonic	Address	R/W	Bits	Description	Default
R_DATA_SLICER_THD	0x0E4[7:0]	RW	8	Data slicer High/Low threshold	0x26
R_DATA_SLICER_START	0x0E5[7:0]	RW	8	Data slicer start point	0x99
R_DATA_SLICER_LINE_E	0x0E6[5:0]	RW	6	Data slicer line select for even field	0x11
R_DATA_SLICER_EN_E	0x0E6[7]	RW	1	Data slicer enable for even field 0: disable 0: enable	1
R_DATA_SLICER_LINE_O	0x0E7[5:0]	RW	6	Data slicer line select for odd field	0x10
R_DATA_SLICER_EN_O	0x0E7[7]	RW	1	Data slicer enable for odd field 0: disable 0: enable	1
R_CC_DATA1_EVEN	0x1C1[7:0]	R	8	Data Slicer First Byte for EVEN Field	-
R_CC_DATA2_EVEN	0x1C2[7:0]	R	8	Data Slicer Second Byte for EVEN Field	-
R_CC_DATA1_ODD	0x1C3[7:0]	R	8	Data Slicer First Byte for ODD Field	-
R_CC_DATA2_ODD	0x1C4[7:0]	R	8	Data Slicer Second Byte for ODD Field	-
R_CC_ERROR	0x1C5[0]	R	1	Data Slicer Error	-
R_CC_INT	0x1C5[1]	R	1	Data Slicer Interrupt	-

6.22.9 Source Detection

BIT1628A 提供 Source Detection 的功能可以自動偵測 AIN11 、AIN12 和 AIN2 何者輸入有信號的變化，偵測的結果將經由 Interrupt 提供系統使用，相關的 Register 設定請參考下表。

Table 6-40 source detection Process Register

Mnemonic	Address	R/W	Bits	Description	Default
R_ADC11_THD	0x0E8[1:0]	RW	2	Signal detection threshold for AIN11	00
R_ADC12_THD	0x0E8[3:2]	RW	2	Signal detection threshold for AIN12	00
R_ADC2_THD	0x0E8[5:4]	RW	2	Signal detection threshold for AIN2	00
R_ADC_SPLIT	0x0E8[7]	RW	1	ADC11/ ADC12 Split Enable 0: Disable 1: Enable	1
R_ADC11_DET_O	0x1C0[0]	R	1	Source detection result for AIN11	-
R_ADC12_DET_O	0x1C0[1]	R	1	Source detection result for AIN12	-
R_ADC2_DET_O	0x1C0[2]	R	1	Source detection result for AIN2 0: No signal toggle 1: Signal toggle	-

6.22.10 AFE and PLL Control

BIT1628A 內建 AFE (Analog Front End) 設定參數，相關設定請參考下表。

Table 6-41 ADC Control Register

Mnemonic	Address	R/W	Bits	Description	Default
R_AFE_CS	0x0E9[1:0]	RW	2	AFE Clamp current	00
R_AFE_CTRPH	0x0E9[3:2]	RW	2	AFE Phase Non-overlap time	00
R_AFE_CTRIB	0x0E9[6:4]	RW	3	AFE Bias current control	000
R_AFE_SH2VCM	0x0E9[7]	RW	1	AFE Internal shortcut on both PGA	0
R_AFE_ENIB	0x0EA[0]	RW	1	AFE Bias current enable	1
R_AFE_ENREF	0x0EA[1]	RW	1	AFE Reference Generator enable	1
R_AFE_ENVBG	0x0EA[2]	RW	1	AFE Bandgap Generator enable	1
R_AFE_ENVCM	0x0EA[3]	RW	1	AFE common mode voltage Generator enable	1
R_AFE_ENAY	0x0EA[4]	RW	1	Power Down Input for ADC1 0: Power Down 1: Normal Operation	1
R_AFE_ENAC	0x0EA[5]	RW	1	Power Down Input for ADC 2 0: Power Down 1: Normal Operation	1
R_AFE_BYP	0x0EA[6]	RW	1	Bypass PGA for ADC test	0
R_AFE_DEC	0x0EA[7]	RW	1	Control output data decimator by 8 or none(dec = 0 : normal operation)	0
R_PLL_POR	0x0EB[0]	RW	1	PLL Power on Reset 0: Disable 1: Reset	0
R_PLL_EAPLL	0x0EB[1]	RW	1	PLL Enable 0: Disable 1: Enable	1
R_PLL_ICP0	0x0EB[2]	RW	1	PLL Factor 0	0
R_PLL_ICP1	0x0EB[3]	RW	1	PLL Factor 1	0
R_POL_YPBPR675	0x0EB[4]	RW	1	YPbPr Mode CLK675 Polarity 0: Normal 1: Invert	0
R_POL_YPBPR135	0x0EB[5]	RW	1	YPbPr Mode CLK135 Polarity 0: Normal 1: Invert	0
R_CLK27_POL	0x0EB[6]	RW	1	Video Clock 27M Polarity 0: Normal 1: Invert	0
R_CLK27_EN	0x0EB[7]	RW	1	Video Clock 27M Enable 0: Disable 1: Enable	1

6.22.11 Standard setting and detection

BIT1628A 可以針對 PAL、PAL60、PAL-N、SECAM、PAL-M、NTSC-443-50、NTSC-M、NTSC-443-60 和 Black&White 等 Color Standard 信號進行解碼，並提供自動、半自動和手動三種模式，以便使用者依據其實際環境進行設定。相關架構示意圖請參考下圖，相關 Register 設定請參考 **Table 6-42**

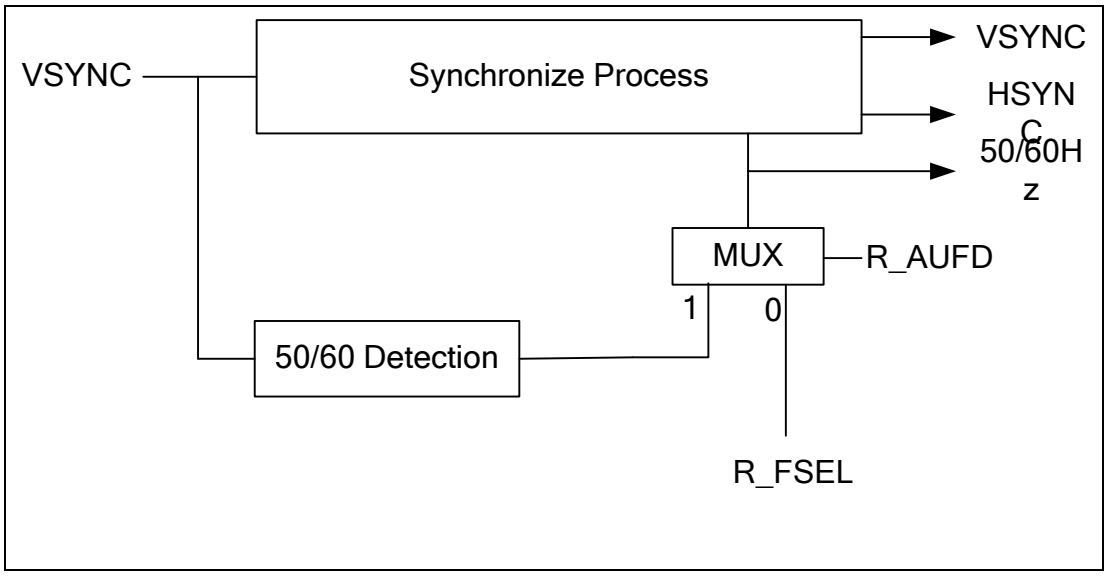


Figure 6-22 Field type select

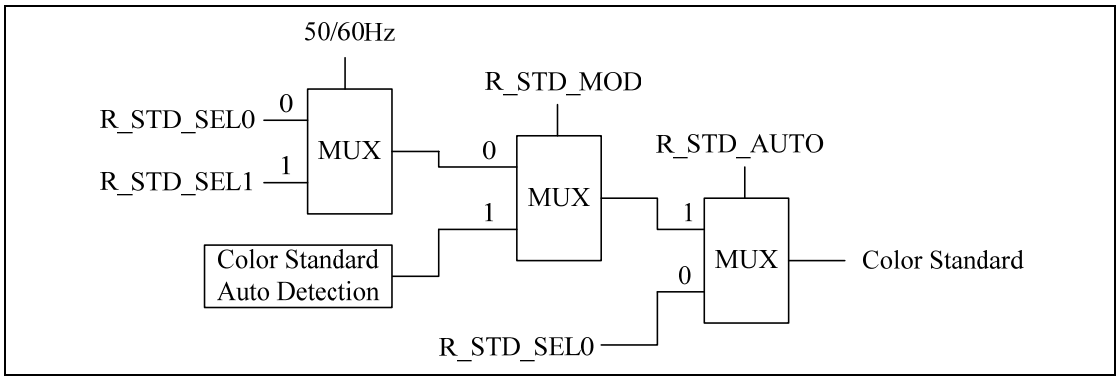


Figure 6-23 Color Standard select

Table 6-42 Standard Setting and Detection Register

Mnemonic	Address	R/W	Bits	Description	Default
R_FSEL	0x0EE[0]	RW	1	Manual 50/60Hz select (R_AUFD=0) 0: 50Hz 1: 60Hz	1
R_AUFD	0x0EE[1]	RW	1	Auto 50/60Hz detection 0: Manual 50/60Hz (Defined on 0x0EE[0]) 1: Auto 50/60Hz detection	0
R_STD_AUTO	0x0ED[7]	RW	1	Color Standard Detect 0: Manual Color Standard (Defined on 0xED[6:4]) 1: Auto Color Standard	0
R_STD_MOD	0x0ED[3]	RW	1	Auto Color Standard Detect Mode Select 0: Semi-Auto Mode 1: Fully-Auto Mode	1
R_STD_SEL0	0x0ED[2:0]	RW	3	Color Standard Setup for Manual Setting and Semi-Auto on 50Hz	101
R_STD_SEL1	0x0ED[6:4]	RW	3	Color Standard Setup for Semi-Auto on 60Hz	101

				000: PAL/PAL-60	
				001: PAL_N	
				010: SECAM	
				011: PAL_M	
				100: NTSC_4.43_50Hz	
				101: NTSC_M / NTSC_J	
				110: NTSC_4.43_60Hz	
				111: Black & White	

6.22.12 Input Path Select

BIT1628A Video Decoder 內建一組 10 Bits ADC，提供 CVBS 的信號輸入，其相關架構示意圖請參考下圖，相關 Register 設定請參考 **Table 6-43**。

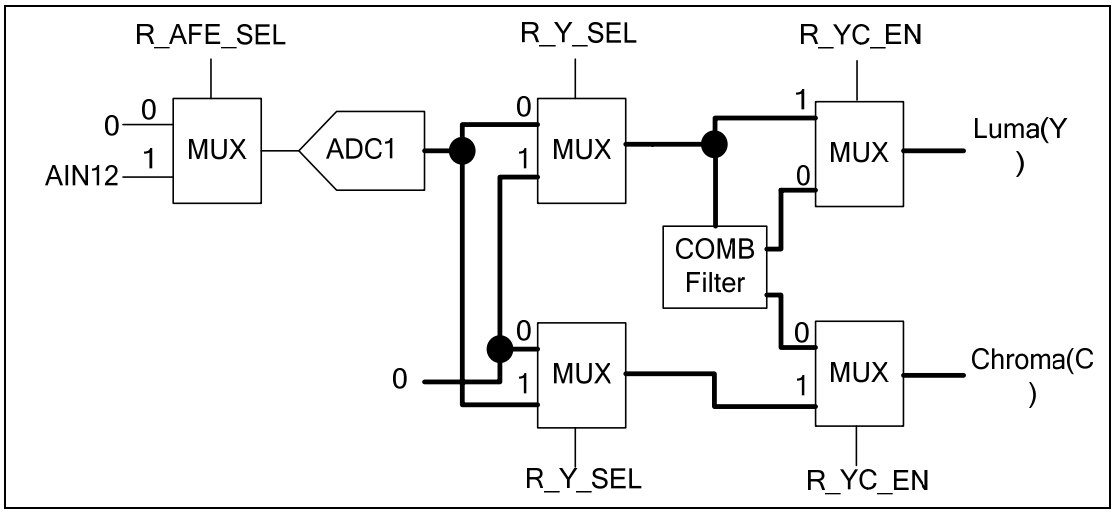


Figure 6-24 Input path

Table 6-43 Analog Input Path Register					
Mnemonic	Address	R/W	Bits	Description	Default
R_Y_SEL	0x0EE[2]	RW	1	Reserve, Set to 1	0
R_YC_EN	0x0EE[3]	RW	1	Reserve, Set to 0	0
R_YCBCR_EN	0x0EE[4]	RW	1	Reserve, Set to 0	0
R_YPBPR_EN	0x0EE[5]	RW	1	Reserve, Set to 0	0
R_AFE_SEL	0x0EE[6]	RW	1	Reserve, Set to 1	0

6.22.13 Video Decoder Status Register

BIT1628A Built-in Video Decoder 提供，下列 Read Only Register，以便讀取 BIT1628A 內部 Status，相關 Register 請參考下表。

Table 6-44 Video Decoder Status Register					
Mnemonic	Address	R/W	Bits	Description	Default
R_DAGC_STABLE_O	0x1AF[0]	R	1	DGC into Stable Mode 0: Tracker Mode 1: Stable Mode	-
R_DAGC_STABLE_VS_O	0x1AF[1]	R	1	DGC into VSYNC Stable Mode 0: Tracker Mode 1: Stable Mode	-
R_DCLAMP_STABLE_O	0x1AF[2]	R	1	DCLAMP into Stable Mode 0: Tracker Mode 1: Stable Mode	-
R_DCLAMP_STABLE_VS_O	0x1AF[3]	R	1	DCLAMP into VSYNC Stable Mode 0: Tracker Mode 1: Stable Mode	-

R_DGAIN1_O	0x1B2[7:6],0x1B0[7:0]	R	10	Digital AGC1 tracer value	-
R_DGAIN2_O	0x1B2[5:4],0x1B1[7:0]	R	10	Digital AGC2 tracer value	-
R_AGAIN1_O	0x1B2[3:2]	R	2	Analog ACG1 tracer value	
R_AGAIN2_O	0x1B2[1:0]	R	2	Analog AGC2 tracer value	
R_DCLAMP11_O	0x1B4[7:0],0x1B3[7:0]	R	16	Digital Clamp 11 tracer value	-
R_DCLAMP12_O	0x1B6[7:0],0x1B5[7:0]	R	16	Digital Clamp 12 tracer value	-
R_DCLAMP2_O	0x1B8[7:0],0x1B7[7:0]	R	16	Digital Clamp 2 tracer value	-
R_STD_GAINOUT_O	0x1BB[7:4],0x1B9[7:0]	R	12	Chroma GAIN tracer value	-
R_STD_PHASEOUT_O	0x1BB[2:0],0x1BA[7:0]	R	11	Chroma Burst Phase tracer value	-
R_COLORDET_O	0x1BB[3]	R	1	Color detection result 0: no color or low color 1: color source	-
R_STD_MODE_O	0x1BC[2:0]	R	3	Color Standard Detection Result 000: PAL 001: PAL_N 010: SECAM 011: PAL_M 100: NTSC_4.43_50Hz 101: NTSC_M / NTSC_J 110: NTSC_4.43_60Hz 111: B&W	-
R_FIDT_O	0x1BC[3]	R	1	50/60Hz detection 0: 50Hz 1: 60Hz	-
R_STD_FREQ	0x1BC[5:4]	R	2	Color Burst Detection 00: 3.57MHz 01: 4.2MHz 10: 4.3 MHz 11: Non-Standard	-
R_STD_READY_O	0x1BC[6]	R	1	Auto Color Standard Detection Ready	-
R_SYNC_READY_O	0x1BC[7]	R	1	Auto Sync Detection Ready	-
R_INCCHRO_O	0x1BF[0],0x1BE[7:0],0x1BD[7:0]	R	17	PLL tracer value	
R_HLCK_O	0x1BF[2]	R	1	H-LOCK Ready 0: Not Ready 1: Ready	-
R_STD_PHASE	0x1BF[3]	R	1	Burst Phase detection 0: 0 – 180 – 0 1: 0 – 90 – 180 – 270 – 0	-
R_SQP_COUNT	0x1BF[7:4]	R	4	Burst phase detection	-
R_MV_DET_SYNC_O	0x1C0[4]	R	1	MV source detection 0: Not MV source 1: MV Source	-
R_MV_DET_CHROMA_O	0x1C0[5]	R	1	MV source on Chroma 0: Not MV Source 1: MV Source	-
R_MV_TYPE_CHROMA_O	0x1C0[6]	R	1	MV type on Chroma 0: Type2 1: Type3	-
R_VTRC_I	0x1C0[7]	R	1	Auto VTRC mode 0: Non-VTRC mode 1: VTRC mode	-

6.23 Pad Type Setup

BIT1628A 輸出的 PAD 可設定爲 Tri-State 輸出，而輸入的 PAD 尚可控制其內建之 Pull-Up or Pull-Down 電阻導通或關閉相關 Register 設定請參考下表。

Table 6-45 Output Tri-State Control Register					
Mnemonic	Address	R/W	Bits	Description	Default
R_ROUT_TRI	0x0FE[0]	RW	1	ROUT Port Tri-State Enable	1
R_GOUT_TRI	0x0FE[1]	RW	1	GOUT Port Tri-State Enable	1
R_BOUT_TRI	0x0FE[2]	RW	1	BOUT Port Tri-State Enable	1
R_TOUT_TRI	0x0FE[3]	RW	1	Reserve, Set to 1	1
R_PWM0_TRI	0x0FE[4]	RW	1	PWM0 pin Tri-State Enable	1
R_PWM1_TRI	0x0FE[5]	RW	1	Reserve, Set to 1	1
R_OCLK_TRI	0x0FE[6]	RW	1	OCLK Pin Tri-State Enable 1 ➔ Tri-State, 0 ➔Normal	1

Table 6-46 Pad Pull Up or Down Control Register					
Mnemonic	Address	R/W	Bits	Description	Default
R_RIN_PD	0x0F1[7:0]	RW	8	RIN[7:0] Port Pull-Down resistance on/off	0x00
R_RIN_PU	0x0F2[7:0]]	RW	8	RIN[7:0] Port Pull-Up resistance on/off	0xFF
R_GIN_PD	0x0F3[7:0]	RW	8	Reserve, Set to 0x00	0x00
R_GIN_PU	0x0F4[7:0]	RW	8	Reserve, Set to 0xFF	0xFF
R_BIN_PD	0x0F5[7:0]	RW	8	Reserve, Set to 0x00	0x00
R_BIN_PU	0x0F6[7:0]	RW	8	Reserve, Set to 0xFF	0xFF
R_HSYNC_PD	0x0F7[4]	RW	1	HSYNC Port Pull-Down resistance on/off	0
R_HSYNC_PU	0x0F7[5]	RW	1	HSYNC Port Pull-Up resistance on/off	1
R_VSYNC_PD	0x0F7[6]	RW	1	VSYNC Port Pull-Down resistance on/off	0
R_VSYNC_PU	0x0F7[7]	RW	1	VSYNC Port Pull-Up resistance on/off 1 ➔ on, 0 ➔off	1

6.24 Multi-Function Pad

BIT1628A 內部提供 3 種工作模式其相關 Register 設定請參考下表。

Table 6-47 Multi-Function Pad Register					
Mnemonic	Address	R/W	Bits	Description	Default
R_OUT_MODE	0x0F7[1:0]	RW	2	Output Mode Select 00: Digital Panel Interface 01: Reserve, Don't use 10: Serial-RGB Interface 11: ITU656 Interface	00
R_PWM0_OUT	0x0F7[2]	RW	1	PWM 0 Output Function Select 0: PWM0 1: Power PWM0	0
R_PWM1_OUT	0x0F7[3]	RW	1	Reserve, Set to 0	0
R_TOUT2_MFP_EN	0x1D5[0]	RW	1	Reserve, Set to 0	0
R_TOUT2_MFP_SEL	0x1D5[1]	RW	1	Reserve, Set to 0	0
R_BIN1_MFP_EN	0x1D5[2]	RW	1	Reserve, Set to 0	0
R_BIN1_MFP_SEL	0x1D5[3]	RW	1	Reserve, Set to 0	0
R_VSYNC_MFP_EN	0x1D5[4]	RW	1	Reserve, Set to 0	0
R_VSYNC_MFP_SEL	0x1D5[5]	RW	1	Reserve, Set to 0	0

6.25 GPO (General Purpose Output) Function

BIT1628A 內部提供 8 個 GPO Register control 輸出、其可分別規劃爲 High Level、Low Level 和 Tri-State 三種狀態。其相關 Register 設定請參考 **Table 6-48**。

Table 6-48 General Purpose Output Register					
Mnemonic	Address	R/W	Bits	Description	Default
R_GPO_SEL	0x0FA[7:0]	RW	8	GPO Port Enable: 0: Disable. 1: Enable.	0x00
R_GPO_TYPE	0x0F9[7:0]	RW	8	GPO Port Type:	0x00

				0: Normal.	
				1: Tri-State.	
R_GPO_REG	0x0F8[7:0]	RW	8	GPO Port Value:	0x00
				0: Low Level.	
				1: High Level.	

6.26 Special Output Setup

BIT1628A 提供 3 組 Special Output Pads (RTS0(Pin30)、RTS1(Pin 31)和 RTS2 (Pin 32))，可經由 Register 分別設定特定輸出功能，其相關設定 Register 及其意義請參考下表。

Table 6-49 Standard Setting and Detection Register

Mnemonic	Address	R/W	Bits	Description				Default
R_RTS0_SEL	0x0FB[3:0]	RW	4	Special Output Pad 0 Function Select				1111
R_RTS1_SEL	0x0FC[3:0]	RW	4	Special Output Pad 1 Function Select				1111
R_RTS2_SEL	0x0FD[3:0]	RW	4	Special Output Pad 2 Function Select				1111
					RTS0	RTS1	RTS2	1111
				0000	HSYNC			
				0001	HREF			
				0010	VSYNC			
				0011	VREF			
				0100	Data Enable			
				0101	EVEN/ODD			
				0110	VD_HC	VD_HSY	VD_HLCK	
				0111	VD_ADC11	VD_ADC12	VD_ADC2	
				1000	MODETYPE			
				1001	AUTOON			
				1010	MCU_BREAK			
				1011	INT1			
				1100	INT0			
				1101	PWM0	PWM1	PWM2	
				1110	IR_Send			
				1111	Tri-State			
R_RTS0_POL	0x0FB[4]	RW	1	Special Output Pad 0 Polarity				0
R_RTS1_POL	0x0FC[4]	RW	1	Special Output Pad 1 Polarity				0
R_RTS2_POL	0x0FD[4]	RW	1	Special Output Pad 2 Polarity				0
				0: Normal				
				1: invert				

6.27 OSD Function

The embedded OSD supports the following features:

1. Three OSD Windows
2. 2048x12 prgrammable OSD Memory
3. Built-in 128 Fixed FONT
4. Index-based Display RAM Memory Management
5. Independent zoom ratio x1~x16 for horizontal direction
6. Independent zoom ratio x1~x16 for vertical direction
7. Programmable Vertical Direction Line Space
8. Programmable Horizontal Character Space
9. Fade IN/OUT Effect
10. 16x2 Color Palette Items (512 colors)
11. Blink display Effect
12. Fringe Font Effect
13. Fringe Window Effect

6.27.1 OSD Windows Function

With the embedded OSD, BIT1628A supports at most 3 OSD windows at the same time; please refer to **Table 6-50** for related registers.

Table 6-50 OSD Windows Register

Mnemonic	Address	R/W	Bits	Description	Default
R_OSD0_X	0x103[5:3], 0x100[7:0]	RW	11	OSD0 start X position	0x00A
R_OSD0_Y	0x103[7:6], 0x101[7:0]	RW	10	OSD0 start Y position	0x00A
R_OSD0_W	0x104[6:0]	RW	7	OSD0 Width (in Characters)	0x00
R_OSD0_H	0x105[5:0]	RW	6	OSD0 Height (in Characters)	0x00
R_OSD1_X	0x113[5:3], 0x110[7:0]	RW	11	OSD1 start X position	0x0D4
R_OSD1_Y	0x113[7:6], 0x111[7:0]	RW	10	OSD1 start Y position	0x00A
R_OSD1_W	0x114[6:0]	RW	7	OSD1 Width (in Characters)	0x0F
R_OSD1_H	0x115[5:0]	RW	6	OSD1 Height (in Characters)	0x07
R_OSD2_X	0x123[5:3], 0x120[7:0]	RW	11	OSD2 start X position	0x000
R_OSD2_Y	0x123[7:6], 0x121[7:0]	RW	10	OSD2 start Y position	0x000
R_OSD2_W	0x124[6:0]	RW	7	OSD2 Width (in Characters)	0x00
R_OSD2_H	0x125[5:0]	RW	6	OSD2 Height (in Characters)	0x00

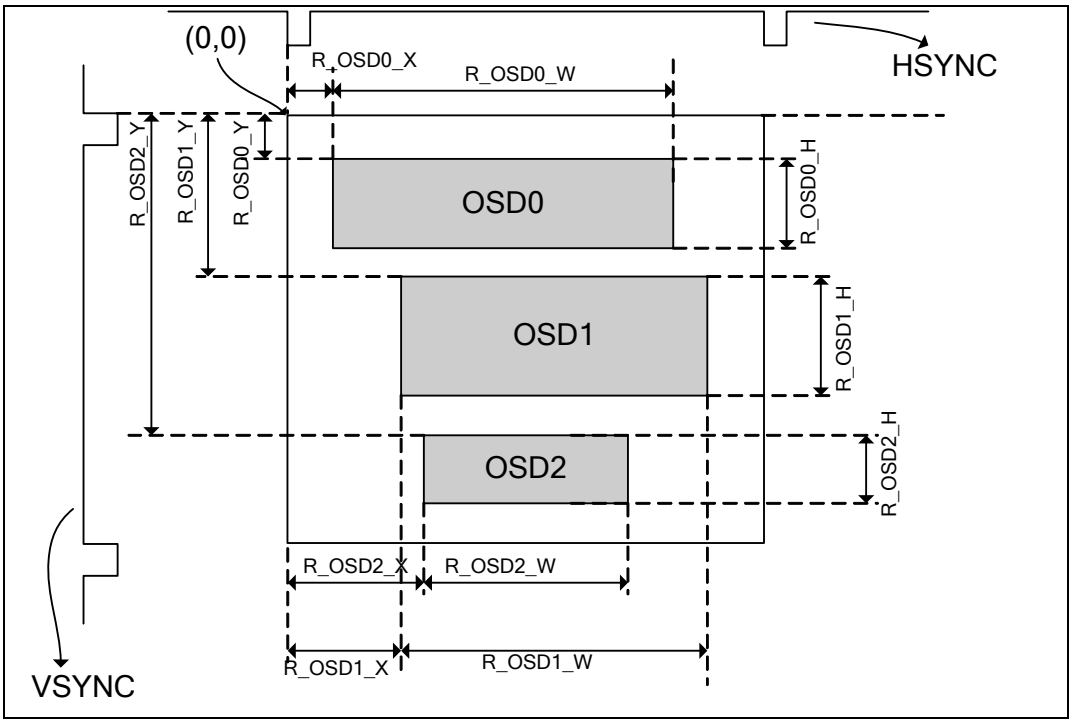


Figure 6-25 OSD Windows Setup

6.27.2OSD Memory Mapping

OSD 的架構如 **Figure 6-25** 所示:

BIT1628A 內建 2048x12 OSD memory 用以作爲儲存 Display、Palette 和 User Font 的資料。存取 OSD Memory 可以經由 Interface Address 300h~4FFh ，並且搭配 register R_OSD_BANKSEL(0x12F[2:0])作爲 Index 以存取 2048x12 的記憶體，每一字節(word)是 12 bits。相關說明請參考下圖。

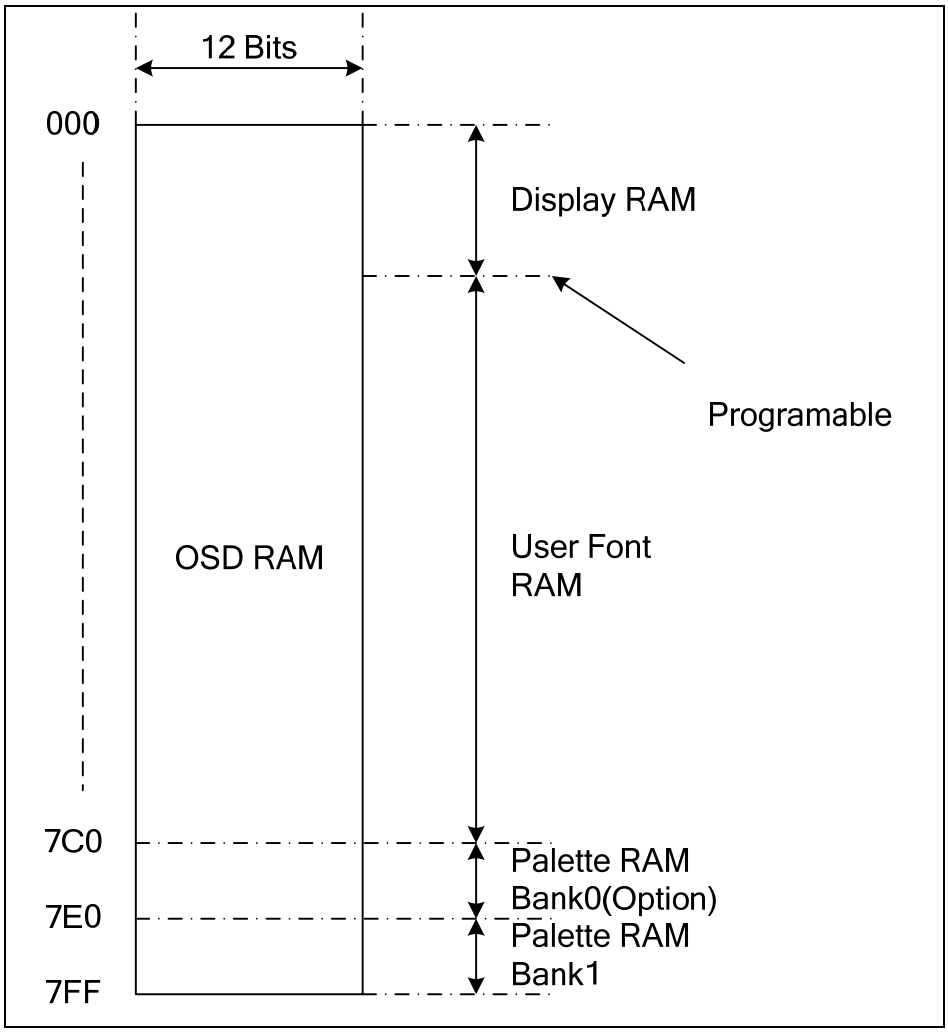
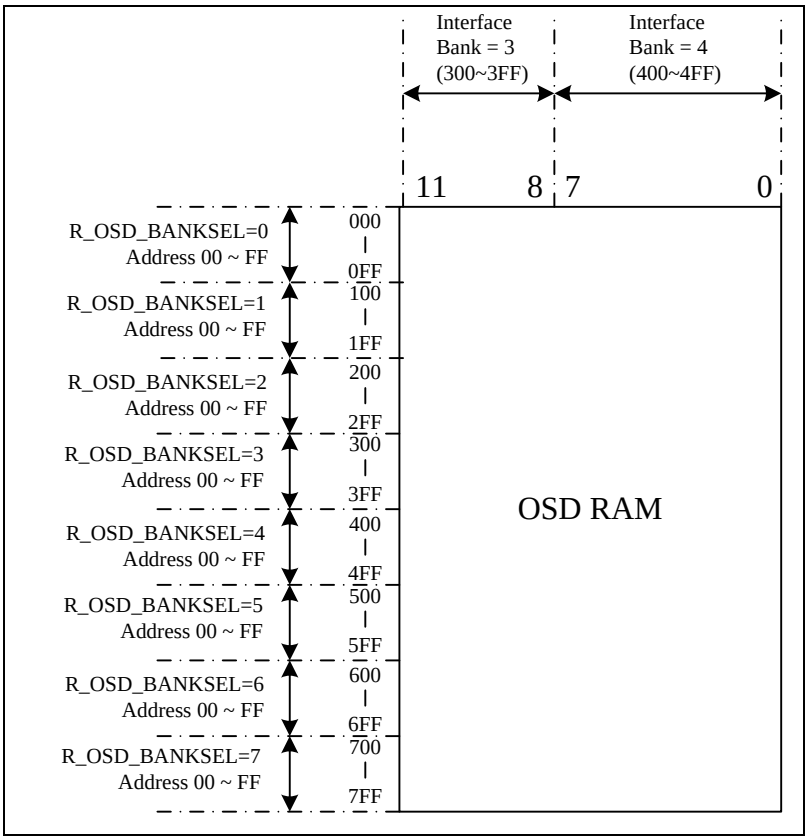
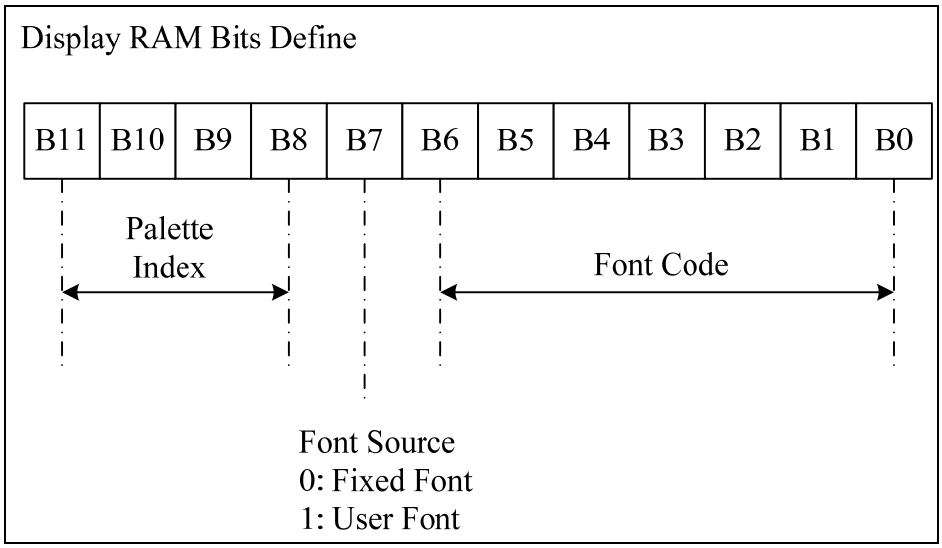


Figure 6-26 OSD Memory Mapping



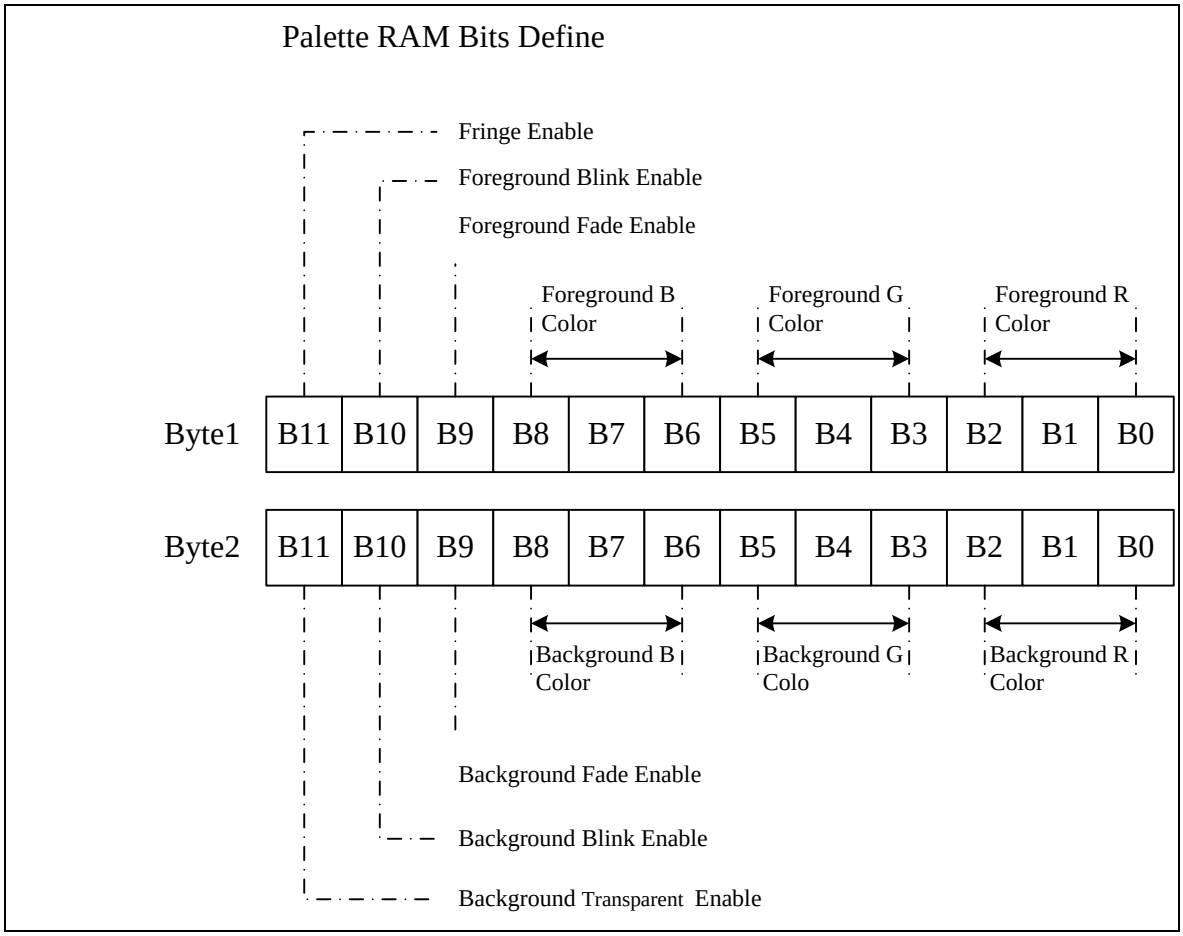
6.27.3Display RAM Definition

BIT1628A OSD 採用 Character based 的方式顯示，每個 Character 的單位爲 12x16 pixels，畫面上要顯示何種 Character 及其屬性是儲存在 Display RAM 內。Display RAM 的格式如下圖所示，分爲 3 個欄位 B6~B0 定義的爲 Font Code，B7 定義爲 Code Source 可設定爲 Fixed Font(ROM)或 User Font(RAM) ，B11~B8 定義爲 Palette Index。



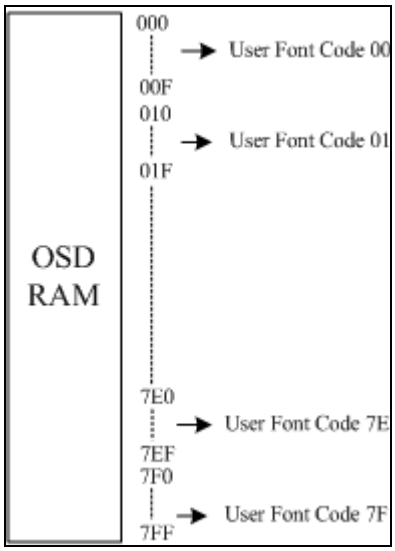
6.27.4Palette RAM Definition

BIT1628A OSD 顯示效果是透過 Palette Table 作爲 Color 及 Attribute mapping 使用，BIT1628A 最多可規劃出兩套的 Palette Table，以 Window 爲單位選擇使用哪一套的 Palette Table。每一個 Palette Table 可設定 16 組 Palettes，可分別設定 Foreground 及 Background 的效果，顯示顏色爲 RGB 各爲 3 bits。相關設定請參考下圖。



6.27.5User Font RAM Definition

BIT1628A OSD User Font 是將整塊的 OSD memory 從 Address 000h 開始以 16 words 爲單位切割爲 128 個 User Font Code，由於 OSD RAM 是 Display RAM 、Palette RAM 和 User Font 共同分享，因此在 User Font 使用上，要避開系統所規劃的 Display 及 Palette RAM 的區域，相關設定請參考下圖。



6.27.6 Color Font RAM Definition

BIT1628A OSD User Font 可以支援 Color Font 的字型，可以 Window 爲單位設定 2 Bits(每個字佔用兩個 User font Code) or 3 Bits(每個字佔用三個 User font Code) Color Font 效果，相關設定請參考下圖。

6.27.7 OSD Windows Attributes

BIT1628A 可以分別爲 3 個 OSD 視窗設定不同的屬性。

Table 6-51 OSD Windows Attribute Register

Mnemonic	Address	R/W	Bits	Description	Default
R_OSD0_INDEXS	{0x103[2:0],0x102[7:0]}	RW	11	OSD0 Display RAM Start index	0x41
R_OSD0_MULX	0x106[3:0]	RW	4	OSD0 Horizontal Character Size 0000: x1, ~ 1111:x16	0000
R_OSD0_MULY	0x106[7:4]	RW	4	OSD0 Vertical Character Size 0000: x1, ~ 1111:x16	0000
R_OSD0_SPCX	0x107[3:0]	RW	4	OSD0 Horizontal Character space	0000
R_OSD0_SPCY	0x107[7:4]	RW	4	OSD0 Vertical Line space	0000
R_OSD0_FRINGE_SEL	0x108[7:0]	RW	8	OSD0 Font Fringe Selection bit7:left,up; bit6:up; bit5:right,up; bit4:left; bit3:right; bit2:left,down; bit1:down; bit0:right,down;	0xFF
R_OSD0_FRINGE_R	0x109[2:0]	RW	3	OSD0 Window Fringe Color R	100
R_OSD0_FRINGE_G	0x109[6:4]	RW	3	OSD0 Window Fringe Color G	010
R_OSD0_FRINGE_B	0x10A[2:0]	RW	3	OSD0 Window Fringe Color B	001
R_OSD0_PATSEL	0x109[7]	RW	1	OSD0 Palette Bank Select 0: Bank0 1: Bank1	1
R_OSD0_FADE_VAL	0x10A[7:4]	RW	4	OSD0 Fade in/out Level	0000
R_OSD0_WX_MIR	0x10B[0]	RW	1	OSD0 Window Mirror for horizontal	0
R_OSD0_WY_MIR	0x10B[1]	RW	1	OSD0 Window Flip	0
R_OSD0_FX_MIR	0x10B[2]	RW	1	OSD0 Characters Mirror for horizontal 0: Mirror 1: Normal	1
R_OSD0_FY_MIR	0x10B[3]	RW	1	OSD0 Characters Mirror for vertical 0: Normal 1: Mirror	0

R_OSD0_BLINK_SEL	0x10B[6:4]	RW	3	OSD0 Blink Period (in VSYNC) 3'b000 : 1; 3'b001 : 2; 3'b010 : 4; 3'b011 : 8; 3'b100 : 16; 3'b101 : 32; 3'b110 : 64; 3'b111 : 128;	000
R_OSD0_EN	0x10B[7]	RW	1	OSD0 Window enable 0: OSD OFF 1: OSD ON	0
R_OSD1_INDEXS	{0x113[2:0],0x112[7:0]}	RW	11	OSD1 Display RAM Start index	
R_OSD1_MULX	0x116[3:0]	RW	4	OSD1 Horizontal Character Size 0000: x1, ~ 1111:x16	0001
R_OSD1_MULY	0x116[7:4]	RW	4	OSD1 Vertical Character Size 0000: x1, ~ 1111:x16	0001
R_OSD1_SPCX	0x117[3:0]	RW	4	OSD1 Horizontal Character space	0000
R_OSD1_SPCY	0x117[7:4]	RW	4	OSD1 Vertical Line space	0000
R_OSD1_FRINGE_SEL	0x118[7:0]	RW	8	OSD1 Font Fringe Selection bit7:left,up; bit6:up; bit5:right,up; bit4:left; bit3:right; bit2:left,down; bit1:down; bit0:right,down;	0x00
R_OSD1_FRINGE_R	0x119[2:0]	RW	3	OSD1 Window Fringe Color R	000
R_OSD1_FRINGE_G	0x119[6:4]	RW	3	OSD1 Window Fringe Color G	000
R_OSD1_FRINGE_B	0x11A[2:0]	RW	3	OSD1 Window Fringe Color B	000
R_OSD1_PATSEL	0x119[7]	RW	1	OSD1 Palette Bank Select 0: Bank0 1: Bank1	1
R_OSD1_FADE_VAL	0x11A[7:4]	RW	4	OSD1 Fade in/out Level	0000
R_OSD1_WX_MIR	0x11B[0]	RW	1	OSD1 Window Mirror for horizontal	0
R_OSD1_WY_MIR	0x11B[1]	RW	1	OSD1 Window Flip	0
R_OSD1_FX_MIR	0x11B[2]	RW	1	OSD1 Characters Mirror for horizontal 0: Mirror 1: Normal	1
R_OSD1_FY_MIR	0x11B[3]	RW	1	OSD1 Characters Mirror for vertical 0: Normal 1: Mirror	0
R_OSD1_BLINK_SEL	0x11B[6:4]	RW	3	OSD1 Blink Period (in VSYNC) 3'b000 : 1; 3'b001 : 2; 3'b010 : 4; 3'b011 : 8; 3'b100 : 16; 3'b101 : 32; 3'b110 : 64; 3'b111 : 128;	000
R_OSD1_EN	0x11B[7]	RW	1	OSD1 Window enable 0: OSD OFF 1: OSD ON	0
R_OSD2_INDEXS	{0x123[2:0],0x122[7:0]}	RW	11	OSD2 Display RAM Start index	0x000
R_OSD2_MULX	0x126[3:0]	RW	4	OSD2 Horizontal Character Size 0000: x1, ~ 1111:x16	0000
R_OSD2_MULY	0x126[7:4]	RW	4	OSD2 Vertical Character Size 0000: x1, ~ 1111:x16	0000
R_OSD2_SPCX	0x127[3:0]	RW	4	OSD2 Horizontal Character space	0000
R_OSD2_SPCY	0x127[7:4]	RW	4	OSD2 Vertical Line space	0000
R_OSD2_FRINGE_SEL	0x128[7:0]	RW	8	OSD2 Font Fringe Selection bit7:left,up; bit6:up; bit5:right,up; bit4:left; bit3:right; bit2:left,down; bit1:down; bit0:right,down;	0x00
R_OSD2_FRINGE_R	0x129[2:0]	RW	3	OSD2 Window Fringe Color R	000
R_OSD2_FRINGE_G	0x129[6:4]	RW	3	OSD2 Window Fringe Color G	000
R_OSD2_FRINGE_B	0x12A[2:0]	RW	3	OSD2 Window Fringe Color B	000
R_OSD2_PATSEL	0x129[7]	RW	1	OSD2 Palette Bank Select	0

				0: Bank0 1: Bank1	
R_OSD2_FADE_VAL	0x12A[7:4]	RW	4	OSD2 Fade in/out Level	0000
R_OSD2_WX_MIR	0x12B[0]	RW	1	OSD2 Window Mirror for horizontal	0
R_OSD2_WY_MIR	0x12B[1]	RW	1	OSD2 Window Flip	0
R_OSD2_FX_MIR	0x12B[2]	RW	1	OSD2 Characters Mirror for horizontal 0: Mirror 1: Normal	1
R_OSD2_FY_MIR	0x12B[3]	RW	1	OSD2 Characters Mirror for vertical 0: Normal 1: Mirror	0
R_OSD2_BLINK_SEL	0x12B[6:4]	RW	3	OSD2 Blink Period (in VSYNC) 3'b000 : 1; 3'b001 : 2; 3'b010 : 4; 3'b011 : 8; 3'b100 : 16; 3'b101 : 32; 3'b110 : 64; 3'b111 : 128;	000
R_OSD2_EN	0x12B[7]	RW	1	OSD2 Window enable 0: OSD OFF 1: OSD ON	0
R_OSD_COLORFONT	0x12E[6:0]	RW	7	OSD Color font index	0x00
R_OSD_COLORBITS	0x12E[7]	RW	1	OSD Color Bits 0: 2 Bits (4 colors) 1: 3 Bits (8 colors)	0
R_OSD_BANKSEL	0x12F[2:0]	RW	3	OSD Memory Bank Select	000

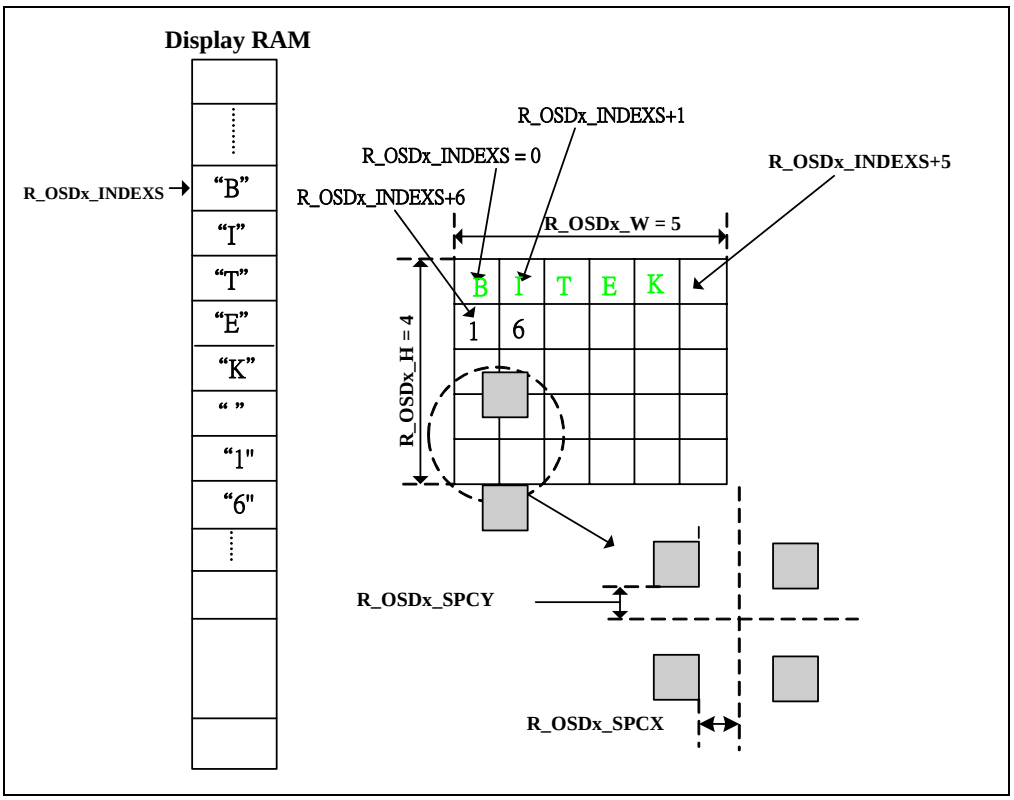


Figure 6-27 OSD Windows Attribute

6.27.8 OSD Built-in Fixed Font

BIT1628A 已內建 128 種 OSD 字型，其定址如下:

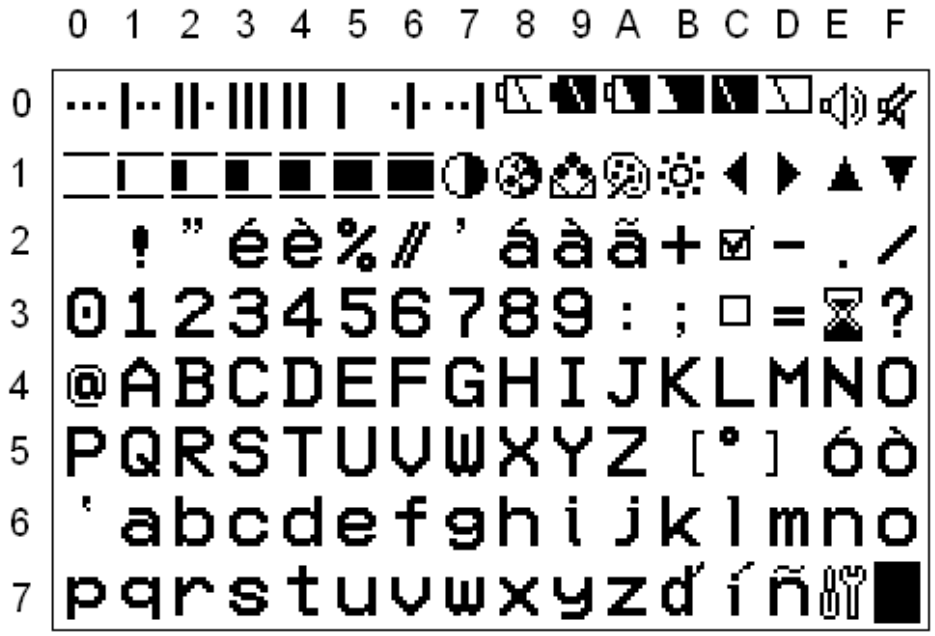


Figure 6-28 Fixed FONT

6.28 EEPROM DMA Mode

BIT1628A 內建 DMA 功能提供在 Master Mode(8051) 模式下，能夠不透過 MCU 逐筆搬移資料，直接將 EEPROM 內的資料直接搬移至 register 內，也可作爲 EEPROM 的介面將資料透過 register 寫入 EEPROM 內。其相關設定 Register 請參考下表：

Table 6-52 EEPROM DMA Register

Mnemonic	Address	R/W	Bits	Description	Default
R_SERIAL_CKEN_SEL	0x130[6:0]	RW	7	EEPROM Clock Select	0x1D
R_EEPROM_TYPE	0x130[7]	RW	1	EEPROM Type Select 0: 24c16 serial 1: 24c32 serial	0
R_SPI_OPCODE	0x131[7:0]	RW	8	SPI Mode OPCODE	0x05
R_DMA_DIN	0x132[7:0]	RW	8	DMA Single Write mode DATA input	0x00
R_DMA_EADDR	0x135[7:0],0x134[7:0],0x133[7:0]	RW	24	DMA EADDR(Storage Address)	0x0000
R_DMA_RADDR	0x137[2:0],0x136[7:0]	RW	10	DMA RADDR(Register Address)	0x000
R_SPI_ADDR_SEL	0x137[5:4]	RW	2	SPI Mode ADDR	00
R_SPI_MODE	0x137[7]	RW	1	SPI Register Mode enable 0: Disable 1: Enable	0
R_DMA_COUNT	0x138[7:0]	RW	8	DMA transfer Count	0x00
R_DMA_MODE	0x139[1:0]	RW	2	DMA transfer Mode 00: Single Write Mode 01: Single Read Mode 1x: Burst Transfer Mode	00
R_DMA_BUS	0x139[2]	RW	1	DMA Bus Select 0: SPI Mode 1: I2C Mode	0
R_DMA_EN	0x139[7]	RW	1	DMA Enable (rising edge) 0: Disable 1: Enable	0
R_DMA_OUT	0x13A[7:0]	R	8	DMA Single Read mode DATA output	-

6.29 IR Decoder Function

BIT1628A 提供 NEC IR Decoder function，由 BIT1628A 偵測 NEC IR Format，並經由 Interrupt 提供給 MCU 參考，其相關設定 Register 請參考下表：

Table 6-53 IR Decoder Register

Mnemonic	Address	R/W	Bits	Description	Default
R_IR_CC	0x13E[7:0]	RW	8	User Defined Customer Code	0x0
	0x13D[7:0]	RW	8	User Defined Customer /Code	000
R_POL_IR	0x13F[0]	RW	1	NEC IR Polarity 0: Normal 1: Invert	0
R_IR_DISREPT	0x13F[1]	RW	1	Repeat Code Detection Enable 0: Enable Repeat Code 1: Disable Repeat Code	0
R_IR_BASE	0x13F[4:2]	RW	3	NEC IR Clock Base 000: XCLK 001: XCLK/2 010: XCLK/3 011: XCLK/4 100: XCLK/5	000

				101: XCLK/6 110: XCLK/7 111: XCLK/8	
R_IR_CHECK	0x13F[7:5]	RW	3	NEC Interrupt Conditions [5]: Check IR Code = ~IR /Code [6]: Check IR Data = ~IR /Data [7]: Check IR Code = User Defined Customer Code and IR /Code = User Defined Customer /Code	000
R_IR_EN	0x140[0]	RW	1	NEC IR Decoder Enable 0: Disable 1: Enable	0
R_IR_DB	0x140[3:2]	RW	2	IR De-Bounce Setup	00
R_IR_SRC	0x140[6:4]	RW	3	Reserve set to 000	000
R_IR_TYPE	0x140[7]	R	1	IR Code Type 0: First Code 1: Repeat Code	-
R_IR_CODE	0x141[7:0]	R	8	NEC IR /Data Byte	-
	0x142[7:0]	R	8	NEC IR /Code Byte	-
	0x143[7:0]	R	8	NEC IR Data Byte	-
	0x144[7:0]	R	8	NEC IR Code Byte	-

6.30 IR Encoder Function

BIT1628A 提供 NEC IR Encoder function，由 BIT1628A RTS0 、RTS1 、RTS2 and PWM0 送出 NEC IR Format 的信號，其相關設定 Register 請參考下表：

Table 6-54 IR Encoder Register

Mnemonic	Address	R/W	Bits	Description	Default
R_IR_SEND_CODE	0x146[7:0]	RW	8	NEC IR /Data Byte	0x00
	0x147[7:0]	RW	8	NEC IR Data Byte	0x00
	0x148[7:0]	RW	8	NEC IR /Code Byte	0x00
	0x149[7:0]	RW	8	NEC IR Code Byte	0x00
R_IR_SEND_REPEAT	0x14A[7:0]	RW	8	Repeat Code Times	0x00
R_IR_SEND_BASE	{0x14C[6:0],0x14B[7:0]}	RW	15	IR base unit (560us) base on XCLK	0x001
R_IR_SEND_EN	0x14C[7]	RW	1	NEC IR Send Enable (pos-edge) 0: Disable 1: Enable	0
R_IR_SEND_SRC	0x14D[2:0]	RW	3	IR Source Select [0] : output to PWM0 [2:1] : Reserve set to 00	000
R_IR_SEND_POL	0x14D[3]	RW	1	IR Send Polarity 0: Normal 1: Invert	0
R_IR_SEND_BUSY	0x14D[7]	R	1	IR Send Status 0: Free 1: Busy	0

6.31 PWM Function

BIT1628A 提供三組可獨立設定之 PWM 輸出，可藉此控制背光、聲音等裝置，其相關設定 Register 請參考下表，相對應之示意圖請參考 **Figure 6-29**：

Table 6-55 PWM Function Register

Mnemonic	Address	R/W	Bits	Description	Default
R_PWM0_FREQ	0x14F[3:0], 0x14E[7:0]	RW	12	PWM0 Output Cycles.	0x100
R_PWM0_REF	0x14F[7:4]	RW	4	PWM0 Reference Cycles.	0x1
R_PWM0_DUTY	0x151[3:0], 0x150[7:0]	RW	12	PWM0 Output Duty Cycle	0x080
R_PWM0_EN	0x152[0]	RW	1	PWM0 Function Enable 0: Disable 1: Enable	0
R_PWM0_POL	0x152[1]	RW	1	PWM0 Output Polarity 0: Normal 1: Invert	0
R_PWM0_SYNC	0x152[3:2]	RW	2	PWM0 synchronized with VSYNC 11: synchronized with input VSYNC 10: synchronized with output VSYNC 0x: no synchronized with VSYNC	11
R_PWM0_INV	0x152[4]	RW	1	PWM1 output select 0: PWM1 signal 1: Invert PWM0 signal	0
R_PWM1_FREQ	0x154[3:0], 0x153[7:0]	RW	12	PWM1Output Cycles.	0x200
R_PWM1_REF	0x154[7:4]	RW	4	PWM1 Reference Cycles.	0x3
R_PWM1_DUTY	0x156[3:0], 0x155[7:0]	RW	12	PWM1 Output Duty Cycle	0x100
R_PWM1_EN	0x157[0]	RW	1	PWM1 Function Enable 0: Disable 1: Enable	0
R_PWM1_POL	0x157[1]	RW	1	PWM1 Output Polarity	0

				0: Normal 1: Invert	
R_PWM1_SYNC	0x157[3:2]	RW	2	PWM1 synchronized with VSYNC 11: Synchronized with input VSYNC 10: Synchronized with output VSYNC 0x: No synchronized with VSYNC	11
R_PWM2_FREQ	0x159[3:0], 0x158[7:0]	RW	12	PWM2 Output Cycles.	0x300
R_PWM2_REF	0x159[7:4]	RW	4	PWM2 Reference Cycles.	0x00
R_PWM2_DUTY	0x15B[3:0], 0x15A[7:0]	RW	12	PWM2 Output Duty Cycle	0x150
R_PWM2_EN	0x15C[0]	RW	1	PWM2 Function Enable 0: Disable 1: Enable	1
R_PWM2_POL	0x15C[1]	RW	1	PWM2 Output Polarity 0: Normal 1: Invert	0
R_PWM2_SYNC	0x15C[3:2]	RW	2	PWM2 synchronized with VSYNC 11: Synchronized with input VSYNC 10: Synchronized with output VSYNC 0x: No synchronized with VSYNC	11

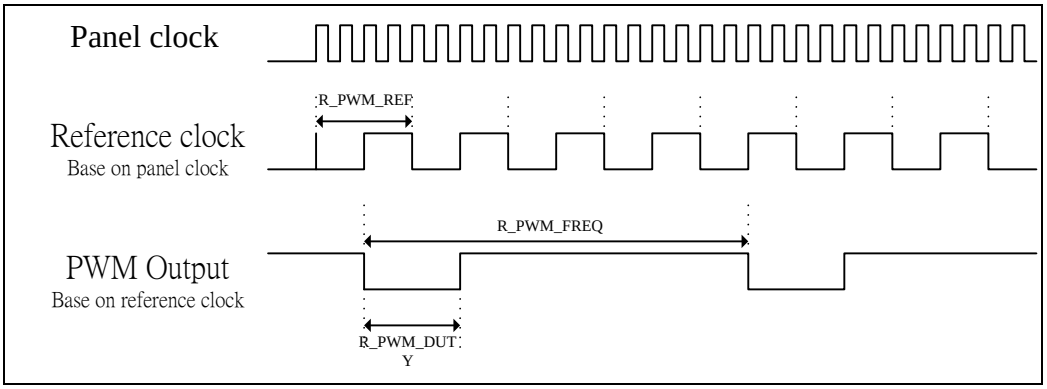


Figure 6-29 PWM Function

6.32 SPI Transfer Function

BIT1628A 內建 SPI Transfer 可用來發送 SPI protocol，相關說明及設定請參考下列圖表。

Table 6-56 SPI Transfer Register

Mnemonic	Address	R/W	Bits	Description	Default
R_SPI_INV	0x15E[2:0]	RW	3	SPI Output Polarity Setup R_SPI_INV[0] : for SPI_SCL setting R_SPI_INV[1] : for SPI_SDA setting R_SPI_INV[2] : for SPI_CS setting 0: Normal 1: Invert	000
R_SPI_SDAM	0x15E[3]	RW	1	SPI_SDA standby status 0: low level 1: High level	0
R_SPI_SCLM	0x15E[5:4]	RW	2	SPI_SCL mode setting R_SPI_SCLM[0] : for CPOL 0: low level	00

				1: high level R_SPI_SCLM[1]: for CPHA 0: rise edge 1: fall edge	
R_SPI_SPEED	0x15E[7:6]	RW	2	SPI Transfer speed 00: XCLK/8 01: XCLK/16 10: XCLK/32 11: XCLK/64	00
R_SPI_DATA	{0x161[7:0],0x160[7:0],0x15F[7:0]}	RW	24	SPI Transfer Data	0
R_SPI_BIT	0x162[4:0]	RW	5	SPI Transfer Bits (0~24)	0
R_SPI_BUSY	0x162[5]	R	1	SPI Status 0: Free 1: Busy	-
R_SPI_SYNC	0x162[6]	RW	1	SPI transfer synchronize with VSYNC 0: Disable 1: Enable	0
R_SPI_EN	0x162[7]	RW	1	SPI Enable/Disable 0: Disable 1: Rise edge to send once	0

6.33 TIMER

BIT1628A 內建之 8051 Timer 可經由設定，決定其外部 timer pin 的輸入信號源，相關說明及設定請參考下列圖表。

Table 6-57 Timer Register

Mnemonic	Address	R/W	Bits	Description	Default
R_T0_BASE	0x163[1:0]	RW	2	Timer0 Count Base: 00: Output HSYNC 01: Output VSYNC 10: Input HSYNC 11: Reserve don't use	00
R_T1_BASE	0x163[3:2]	RW	2	Timer1 Count Base: 00: Output HSYNC 01: Output VSYNC 10: Input HSYNC 11: Reserve don't use	00
R_T2_BASE	0x163[5:4]	RW	2	Timer2 Count Base: 00: Output HSYNC 01: Output VSYNC 10: Input HSYNC 11: Reserve don't use	00
R_T22_BASE	0x163[7:6]	RW	2	Timer2 capture count Base: 00: Output HSYNC 01: Output VSYNC 10: Input HSYNC 11: Reserve don't use	00

6.34 GPI and KEY Function

BIT1628A 內建 5 組 GPI (General Purpose Input)，並可針對各個 GPI PIN 分別規劃爲 Level Status，Key Down 或 Key Up 三種觸發狀態，且可經由 Interrupt、KEY_STATUS、KEY_FLAG 及 KEY_LONG 讀回其狀態。相關設定 Register 請參考 **Table 6-58**。

Table 6-58 GPI and KEY Register

Mnemonic	Address	R/W	Bits	Description	Default

R_KEY_SRC0	0x164[7:0]	RW	8	Key input Source Select								0x00
R_KEY_SRC1	0x165[7:0]	RW	8		B7	B6	B5	B4	B3	B2	B1	B0	0x00
				00	RIN7	Reserve		RIN4	RIN3	RIN2	Reserve		
				01	Reserve Don't use								
				10	Reserve Don't use								
				11	Reserve Don't use							HSYNC	
R_KEY_ACK	0x166[7:0]	RW	8	Key detect function Enable / Disable 0: Disable 1: Enable									0xFF
R_KEY_POL	0x167[7:0]	RW	8	Key Source Polarity 0: Normal 1: Invert									0x00
R_KEY_TYPE0	0x168[7:0]	RW	8	Key Detect Type select									0x00
R_KEY_TYPE1	0x169[7:0]	RW	8	00: Falling or Long Key 01: Rising or Long Key 10: Value Changed 11: Long Key only									0x00
R_KEY_LONG_EN	0x16A[7:0]	RW	8	Long Key detect enable 0: Disable 1: Enable									0x00
R_KEY_LONG_SEL	0x16B[7:0]	RW	8	Long Key detect type 0: Falling edge 1: Rising edge									0x00
R_KEY_LONG_TIME	0x16C[4:0]	RW	5	Long Key detect time									0x1F
R_KEY_DB	0x16C[7:5]	RW	3	De-bounce time									000
R_KEY_FLAG	0x16D[7:0]	R	8	Key detect status									-
R_KEY_STATUS	0x16E[7:0]	R	8	Key real time status									-
R_KEY_LONG	0x16F[7:0]	R	8	Long Key status									-

6.35 PLL and OSC Pads

BIT1628A 內建一組 PLL，並依據 Oscillator 所提供的頻率產生可程式化的 Clock 輸出。其相關公式及 Register 請參考 **Table 6-59**。

Table 6-59 PLL Register

Mnemonic	Address	R/W	Bits	Description	Default
R_PLL_PD	0x178[0]	RW	1	PLL Power Down Enable 0: Normal 1: Disable	0
R_PLL_RESETN	0x178[1]	RW	1	PLL Reset 0: Reset 1: Normal	0
R_PLL_HALFCK	0x178[2]	RW	1	PLL Half Clock output 0: Normal 1: Half Clock	0
R_PLL_SEL	0x178[3]	RW	1	PLL Clock Control 0: Normal 1: DIV ((R_PLL_DP+1)*2)	0
Auto switch mode 0 input widows setup					
R_PLL_DM_M0	0x179[4:0]	RW	5	PLL DM Value.	0x00
R_PLL_DN_M0	0x17A[6:0]	RW	7	PLL DN Value.	0x00
R_PLL_DP_M0	0x17B[5:0]	RW	6	PLL DP Value.	0x00
Auto switch mode 1 input widows setup					
R_PLL_DM_M1	0x17C[4:0]	RW	5	PLL DM Value.	0x00
R_PLL_DN_M1	0x17D[6:0]	RW	7	PLL DN Value.	0x00
R_PLL_DP_M1	0x17E[5:0]	RW	6	PLL DP Value.	0x00

$$PLL\_OUT = \frac{(R\_PLL\_DN+1)}{(R\_PLL\_DM+1)} * \frac{1}{2^{R\_PLL\_HALFCK}} * \frac{1}{((R\_PLL\_DP+1)*2)^{R\_PLL\_SEL}} OSC\_Freq\_Sel$$

Figure 6-30 PLL Frequency formula

6.36 Color Information Detection

BIT1628A 內建 Color information Detect function 可以計算在所設定的偵測區域內的 average color information 相關設定請參考下表。

Table 6-60 Color Information Register

Mnemonic	Address	R/W	Bits	Description	Default
R_CORINFO_XS	0x182[3:0], 0x180[7:0]	RW	12	Color detection Window horizontal Start Position	0x000
R_CORINFO_XW	0x182[7:4], 0x181[7:0]	RW	12	Color detection Window horizontal End Position	0x000
R_CORINFO_YS	0x185[2:0], 0x183[7:0]	RW	11	Color detection Window vertical Start Position	0x000
R_CORINFO_YW	0x185[6:4], 0x184[7:0]	RW	11	Color detection Window vertical End Position	0x000
R_CORINFO_Y	0x186[7:0]	R	8	Color detection Y information	-
R_CORINFO_U	0x187[7:0]	R	8	Color detection U information	-
R_CORINFO_V	0x188[7:0]	R	8	Color detection V information	-

6.37 Power PWM Function

BIT1628A 提供一組可獨立設定之 Feedback PWM 輸出，可經由外部輸入之 Feedback 信號，自動調整 PWM Duty 可藉此控制背光、聲音等裝置，其相關設定 Register 請參考下表

Table 6-61 Power PWM Function Register

Mnemonic	Address	R/W	Bits	Description	Default
R_PPWM0_FREQ	0x190[7:0]	RW	8	Power PWM0 Output Cycles.	0xFF
R_PPWM0_DUTY	0x191[7:0]	RW	8	Power PWM0 Output Duty Cycle	0x80
R_PPWM0_HIGH	0x192[7:0]	RW	8	Power PWM0 Duty Maximum	0xF0
R_PPWM0_LOW	0x193[7:0]	RW	8	Power PWM0 Duty Minimum	0x10
R_PPWM0_DB	0x194[2:0]	RW	3	Power PWM0 Feedback signal de-bounce setting	000
R_PPWM0_FBSEL	0x194[3]	RW	1	Power PWM0 Feedback Select 0: from SARADC compare 1: from RIN[0]	0
R_PPWM0_FB	0x194[4]	RW	1	Power PWM0 Feedback enable 0: Disable (Free run Mode) 1: Enable (Tracker Mode)	1
R_PPWM0_POL	0x194[5]	RW	1	Power PWM0 Output Polarity 0: Normal 1: Invert	0
R_PPWM0_SYNC	0x194[6]	RW	1	Power PWM0 synchronized with VSYNC 0: Disable 1: Enable	0
R_PPWM0_EN	0x194[7]	RW	1	Power PWM0 Enable 0: Disable 1: Enable	0
R_PPWM1_EN	0x199[7]	RW	1	Reserve set to 0	0

6.38 ADC Data Interface

BIT1628A 內建 ADC Detect 功能可偵測 SARADC 或 AFE ADC 的 raw data，當輸入的信號有更動時，會發出 Interrupt 提供給使用者應用，其相關設定 Register 請參考下表

Table 6-62 ADC Data interface Register

Mnemonic	Address	R/W	Bits	Description	Default
R_ADC_THD	0x19A[7:0]	RW	8	ADC value change Threshold	0x00
R_ADC_DB	0x19B[2:0]	RW	3	ADC Low Pass Filter Threshold	000
R_ADC_SEL	0x19B[4:3]	RW	2	ADC Source Select 00: ADC11 input 01: ADC12 input 10: ADC2 input 11: SAR ADC input	11
R_ADC_SUBSEL	0x19B[6:5]	RW	2	SARADC Mode Source Select 00: SARADC1 01: SARADC2 10: SARADC3 11: SARADC4	00
R_ADC_COMP	{0x19C[7:0],0x19D[3:0]}	RW	12	ADC detect base value	
R_ADC_LPF_I	0x19E[7:0],0x19F[3:0]	R	12	ADC raw data (low pass filter process)	-
R_ADC11	0x1C6[7:0],0x1C9[1:0]	R	10	ADC raw data (ADC11 Channel)	-
R_ADC12	0x1C7[7:0],0x1C9[3:2]	R	10	ADC raw data (ADC12 Channel)	-
R_ADC2	0x1C8[7:0],0x1C9[5:4]	R	10	ADC raw data (ADC2 Channel)	-

6.39 Auto Detection

BIT1628A 提供七種輸入訊號偵測機制，分別爲 PCLK base SYNC Detection、XCLK base SYNC Detection、Mode Change Detection、Mode Type Detection、 Even/Odd Type Detection、Data Enable Detection 和 No signal Detection。

1. PCLK base SYNC Detection:
   以 PCLK 偵測 External HSYNC、External VSYNC Low Pulse Width 及 Total SYNC Width，其主要作爲 SYNC 極性判別及模式的偵測，此偵測機制 Power On 時就會自動啓動且無法由 MCU 去終止或啓動，其操作步驟如下：
   (讀取偵測 SYNC 資料:)
   Register (0x1A0[7:0]): HSYNC Low pulse (in PCLK)。
   Register (0x1A4[7:4], 0x1A1[7:0]): HSYNC Total width (in PCLK)。
   Register (0x1A2[6:0]): VSYNC Low pulse (in HSYNC)。
   Register (0x1A4[2:0], 0x1A3[7:0]): VSYNC Total width (in HSYNC)。
2. XCLK base HSYNC Detection:
   以 XCLK 偵測 External HSYNC，其主要作爲模式的判別。此偵測機制會以 XCLK 爲基準計算 Input HSYNC Low Level Width 和 HSYNC High Level Width，其操作步驟如下：
   (讀取偵測 SYNC 資料:)
   Register (0x1AA[7:4], 0x1A8[7:0]): HSYNC High Level Width (in XCLK)
   Register (0x1AA[3:0], 0x1A9[7:0]: HSYNC Low Level Width (in XCLK)
3. Mode Change Detection:
   偵測 VSYNC 變化量，如果 VSYNC 變化量大於 8 條 HSYNCs，將會經由 Interrupt 機制回應給 MCU 得知，其操作步驟如下：
   Set Interrupt Enable (Register: 0x04[2])。
   如果 VSYNC 變化量大於 8，將會由 INT Pin 發出 Interrupt，亦可藉由輪詢的方式讀取 Interrupt Flag (Register:0x02[2]) 而得知。
4. Mode Type Detection:
   自動辨別 NTSC/PAL Mode 並可由 Register(0x1AB[1]) 直接讀出其狀態。
5. EVEN/ODD Type Detection:
   自動判別 VSYNC 是否有 EVEN/ODD 相關變化，並可由 Register(0x1AB[2]) 直接讀出其狀態。
6. Data Enable signal Detection:

自動偵測 Data Enable Signal Information 以供系統作爲設定 Input windows 的參考。

7. No signal Detection:
自動判別 HSYNC 是否有 Toggle，如果在 2047 XCLKs 內沒有變化將由 Interrupt (0x02[1:0]) 回應或可由 Register (0x1AB[3])直接讀出其狀態。

Table 6-63 Auto Detection Register

Mnemonic	Address	R/W	Bits	Description	Default
R_IS_XP	0x1A0[7:0]	R	8	HSYNC Low pulse (Base on PCLK)	-
R_IS_XT	0x1A4[7:4], 0x1A1[7:0]	R	12	HSYNC Total width (Base on PCLK)	-
R_IS_YP	0x1A2[7:0]	R	8	VSYNC Low pulse (Base on HSYNC)	-
R_IS_YT	0x1A4[2:0], 0x1A3[7:0]	R	11	VSYNC Total width (Base on HSYNC)	-
R_DE_H	0x1A7[2:0],0x1A5[7:0]	R	11	Data Enable HSYNC Total Width	-
R_DE_V	0x1A7[5:4],0x1A6[7:0]	R	10	Data Enable VSYNC Total Lines	-
R_DET_XP	0x1AA[7:4],0x1A8[7:0]	R	12	HSYNC High Level width (Base on PCLK)	-
R_DET_XN	0x1AA[3:0],0x1A9[7:0]	R	12	HSYNC Low Level width (Base on PCLK)	-
R_MODECHG	0x1AB[0]	R	1	Mode Change Status ➔0: No mode change ➔1: VSYNC 變動量大於 8 HSYNCs	-
R_MODE_TYPE	0x1AB[1]	R	1	Mode Status ➔ 0: 50Hz ➔ 1: 60Hz	-
R_EVENSAME	0x1AB[2]	R	1	EVEN Type status ➔ 0: Had EVEN/ODD information ➔ 1: No EVEN/ODD information	-
R_SIGIN	0x1AB[3]	R	1	Sync Status ➔0: No Signal ➔1: Signal Ready	-
R_AUTOON	0x1AB[4]	R	1	Auto on Status ➔ 0: Normal Mode ➔ 1: Free run Mode	-
R_SWITCH	0x1AB[5]	R	1	Auto Switch Status ➔ 0: Mode 0 ➔ 1: Mode 1	-
R_IEVEN	0x1AB[6]	R	1	Input EVEN/ODD Information ➔ 0: EVEN Field ➔ 1: ODD Field	-
R_OEVEN	0x1AB[7]	R	1	Output EVEN/ODD Information ➔ 0: EVEN Field ➔ 1: ODD Field	-
R_LINEBUF_COUNT	0x1AD[5:.0],0x1AC[7:0]	R	14	Line buffer status	-
R_LINEBUF_ERR_TYPE	0x1AD[6]	R	1	Line buffer Error Status 0: Error Status 0 1: Error Status 1	-
R_LINEBUF_ERR_DET	0x1AD[7]	R	1	Line buffer timing Error 0: No Error 1: Error	-

6.40 ADC Compare Function

BIT1628A 可利用 SARADC 模擬 compare 功能已控制 Power feedback PWM，相關說明及設定請參考下列圖

表。

Table 6-64 ADC compare Register					
Mnemonic	Address	R/W	Bits	Description	Default
R_ADC_HIGH	{0x1CC[7:0],0x1CE[1:0]}	RW	10	High Level threshold	3FF
R_ADC_LOW	{0x1CD[7:0],0x1CE[3:2]}	RW	10	Low Level threshold	000
R_COMP_POL	0x1CE[4]	RW	1	Compare output polarity 0: Normal 1: Invert	0
R_COMP_SEL	0x1CE[6:5]	RW	2	ADC Compare source select 00: SARADC1 01: SARADC2 10: SARADC3 11: SARADC4	00

6.41 SAR ADC

BIT1628A 內建 12 Bits SAR ADC 最多可提供三組的 ADC 輸入，並且內建自動輪詢功能可以分時的方式自動同時偵測 4 個輸入變化，其相關設定 Register 請參考下表

Table 6-65 SARADC Register					
Mnemonic	Address	R/W	Bits	Description	Default
R_SARCLK_DIV	0x009[7:0]	RW	8	SAR ADC clock factor (256-R_SARCLK_DIV clocks base on OSCCLK)	0x20
R_SARCLK_EN	0x00A[0]	RW	1	SAR ADC Clock enable 0: Disable 1: Enable	1
R_SARCLK_POL	0x00A[1]	RW	1	SAR ADC Clock Polarity 0: Normal 1: Invert	0
R_SARADC_EN	0x00A[2]	RW	1	SAR ADC enable 0: Disable 1: Enable	1
R_SARADC_SLEEP	0x1D7[0]	RW	1	Power down signal, high active	0
R_SARADC_LOWSPEED	0x1D7[1]	RW	1	Slows down the SAR when used in low speed mode to save power. High active. High: 200KHz mode; Low: 1MHz	0
R_SARADC_RDB	0x1D7[2]	RW	1	ADC output enable signal. When it has a high to low transition, INTRB will be cleared.	1
R_SARADC_WRB	0x1D7[3]	RW	1	ADC start signal, ADC will be started by a low to high transition.	1
R_REF_SEL_L	0x1D7[5:4]	RW	2	ADC LOW analog reference selection signals: 00: AGND33 01: Reserve don't use 10: Reserve don't use 11: AGND33	11
R_REF_SEL_H	0x1D7[7:6]	RW	2	ADC HIGH analog reference selection signals: 00: Reserve don't use 01: Reserve don't use 10: Reserve don't use 11: AVDD33	11
R_YP_O	0x1D8[0]	RW	1	Reserve set to 0	0

R_XP_O	0x1D8[1]	RW	1	Reserve set to 0	0
R_YM_O	0x1D8[2]	RW	1	Reserve set to 0	0
R_XM_O	0x1D8[3]	RW	1	Reserve set to 0	0
R_YP_C	0x1D8[4]	RW	1	Reserve set to 0	0
R_XP_C	0x1D8[5]	RW	1	Reserve set to 0	0
R_YM_C	0x1D8[6]	RW	1	Reserve set to 0	0
R_XM_C	0x1D8[7]	RW	1	Reserve set to 0	0
R_SARADC1_INSEL	0x1D9[2:0]	RW	3	ADC analog input1 selection signals:	010
R_SARADC2_INSEL	0x1D9[5:3]	RW	3	ADC analog input2 selection signals:	010
R_SARADC3_INSEL	0x1DA[2:0]	RW	3	ADC analog input3 selection signals:	010
R_SARADC4_INSEL	0x1DA[5:3]	RW	3	ADC analog input4 selection signals: 000: Reserve don't use 001: VHS 010: A_2 011: A_3 100: Reserve don't use 101: Reserve don't use 110: Reserve don't use 111: Reserve don't use	010
R_SARADC_MODE	0x1D9[7:6]	RW	2	ADC input mode select 0x: Single Mode refer R_SARADC1_INSEL 10: Two Source Mode Refer R_SARADC1_INSEL and R_SARADC2_INSEL 11: Four Source Mode	00
R_SARADC_SWITCH	0x1DB[7:0]	RW	8	Switch time	
R_SARADC1_I	0x1DC[7:0],0x1E0[3:0]	R	12	ADC switch data (SARADC1)	-
R_SARADC2_I	0x1DD[7:0],0x1E0[7:4]	R	12	ADC switch data (SARADC2)	
R_SARADC3_I	0x1DE[7:0],0x1E1[3:0]	R	12	ADC switch data (SARADC3)	
R_SARADC4_I	0x1DF[7:0],0x1E1[7:4]	R	12	ADC switch data (SARADC4)	
R_SARADC_I	0x1E2[7:0],0x1E3[3:0]	R	12	ADC raw data	
R_SARADC_INTRB	0x1E3[4]	R	1	ADC output data ready, low active.	-
R_SARADC_EOC	0x1E3[5]	R	1	Output data ready	-

7 User Interface

BIT1628A 提供二種 Interface Mode (Slave Mode 和 Master Mode)，使其能應用在不同的環境中。

7.1 Options Pins

BIT1628A 使用 4 根外部 PIN 來做 Mode 的選擇。主要可以分爲 Master 與 Slave Mode。Slave Mode 下，外部的 MCU 可以經由 PIN OP1、OP0 透過 Two-Wire Serial Interface (TWSI) Protocol 控制 BIT1628A。Master Mode 則是運用 BIT1628A 內建 CPU 搭配外部程式記憶體完成系統設計。在 Master Mode 下 8051 MCU 可將程式碼擺放在 24 系列的 Serial EEPROM 內，並透過內建之 8051 MCU 執行即可完成 BIT1628A 的相關控制。

8051 MCU Boot 支援二種記憶體模式，分別是 24C16 系列與 24C32 系列。定義及使用方法請參考下表。

Table 7-1 Options Pins Setup

OP5	OP3	OP1	OP0	Mode
0	0	SCL	SDA	EEPROM 24C16 Boot master mode
0	1	SCL	SDA	EEPROM 24C32 Boot master mode
1	0	SCL	SDA	TWSI Mode Slave Address (0x80~0x8F)
1	1	SCL	SDA	TWSI Mode Slave Address (0xC0~0xCF)

7.2 Master Mode – 8051 MCU

BIT1628A 內建 8051 MCU，可提供使用者將程式碼儲存在 Serial EEPROM 中，BIT1628A 將會依據使用者所撰寫的程式碼內容，解碼後執行其相對的指令。

7.2.1 Instruction Set

BIT1628A 內建 8051 MCU 提供下列的指令碼，相對應的 Instruction Set 與 Instruction Format，請參考。

Mnemonic	Description	Bytes	Bytes Cycles	Bytes Cycles Hex code
ARITHMETIC				
ADD A,Rn	Add register to A	1	1	28-2F
ADD A,dir	Add direct byte to A	2	1	25
ADD A,@Ri	Add indirect memory to A	1	1	26-27
ADD A,#data	Add immediate to A	2	1	24
ADDC A,Rn	Add register to A with carry	1	1	38-3F
ADDC A,dir	Add direct byte to A with carry	2	1	35
ADDC A,@Ri	Add indirect memory to A with carry	1	1	36-37
ADDC A,#data	Add immediate to A with carry	2	1	34
SUBB A,Rn	Subtract register from A with borrow	1	1	98-9F
SUBB A,dir	Subtract direct byte from A with borrow	2	1	95
SUBB A,@Ri	Subtract indirect memory from A with borrow	1	1	96-97
SUBB A,#data	Subtract immediate from A with borrow	2	1	94
INC A	Increment A	1	1	4
INC Rn	Increment register	1	1	08-0F
INC dir	Increment direct byte	2	1	5
INC @Ri	Increment indirect memory	1	1	40336

DEC A	Decrement A	1	1	14
DEC Rn	Decrement register	1	1	18-1F
DEC dir	Decrement direct byte	2	1	15
DEC @Ri	Decrement indirect memory	1	2	16-17
INC DPTR	Increment data pointer	1	4	A3
MUL AB	Multiply A by B	1	4	A4
DIV AB	Divide A by B	1	1	84
DA A	Decimal Adjust A	1	1	D4
LOGICAL				
ANL A,Rn	AND register to A	1	1	58-5F
ANL A,dir	AND direct byte to A	2	1	55
ANL A,@Ri	AND indirect memory to A	1	1	56-57
ANL A,#data	AND immediate to A	2	1	54
ANL dir,A	AND A to direct byte	2	1	52
ANL dir,#data	AND immediate to direct byte	3	2	53
ORL A,Rn	OR register to A	1	1	48-4F
ORL A,dir	OR direct byte to A	2	1	45
ORL A,@Ri	OR indirect memory to A	1	1	46-47
ORL A,#data	OR immediate to A	2	1	44
ORL dir,A	OR A to direct byte	2	1	42
ORL dir,#data	OR immediate to direct byte	3	2	43
XRL A,Rn	Exclusive-OR register to A	1	1	68-6F
XRL A,dir	Exclusive-OR direct byte to A	2	1	65
XRL A, @Ri	Exclusive-OR indirect memory to A	1	1	66-67
XRL A,#data	Exclusive-OR immediate to A	2	1	64
XRL dir,A	Exclusive-OR A to direct byte	2	1	62
XRL dir,#data	Exclusive-OR immediate to direct byte	3	2	63
CLR A	Clear A	1	1	E4
CPL A	Complement A	1	1	F4
SWAP A	Swap Nibbles of A	1	1	C4
RL A	Rotate A left	1	1	23
RLC A	Rotate A left through carry	1	1	33
RR A	Rotate A right	1	1	03
RRC A	Rotate A right through carry	1	1	13
DATA TRANSFER				
MOV A,Rn	Move register to A	1	1	E8-EF
MOV A,dir	Move direct byte to A	2	1	E5

MOV A,@Ri	Move indirect memory to A	1	1	E6-E7
MOV A,#data	Move immediate to A	2	1	74
MOV Rn,A	Move A to register	1	1	F8-FF
MOV Rn,dir	Move direct byte to register	2	2	A8-AF
MOV Rn,#data	Move immediate to register	2	1	78-7F
MOV dir,A	Move A to direct byte	2	1	F5
MOV dir,Rn	Move register to direct byte	2	2	88-8F
MOV dir,dir	Move direct byte to direct byte	3	2	85
MOV dir,@Ri	Move indirect memory to direct byte	2	2	86-87
MOV dir,#data	Move immediate to direct byte	3	2	75
MOV @Ri,A	Move A to indirect memory	1	1	F6-F7
MOV @Ri,dir	Move direct byte to indirect memory	2	2	A6-A7
MOV @Ri,#data	Move immediate to indirect memory	2	1	76-77
MOV DPTR,#data	Move immediate to data pointer	3	2	90
MOVC A,@A+DPTR	Move code byte relative DPTR to A	1	2	93
MOVC A,@A+PC	Move code byte relative PC to A	1	2	83
MOVX A,@Ri	Move external data(A8) to A	1	2	E2-E3
MOVX A,@DPTR	Move external data(A16) to A	1	2	E0
MOVX @Ri,A	Move A to external data(A8)	1	2	F2-F3
MOVX @DPTR,A	Move A to external data(A16)	1	2	F0
PUSH dir	Push direct byte onto stack	2	2	C0
POP dir	Pop direct byte from stack	2	2	D0
XCH A,Rn	Exchange A and register	1	1	C8-CF
XCH A,dir	Exchange A and direct byte	2	1	C5
XCH A,@Ri	Exchange A and indirect memory	1	1	C6-C7
XCHD A,@Ri	Exchange A and indirect memory nibble	1	1	D6-D7
BOOLEAN				
CLR C	Clear carry	1	1	C3
CLR bit	Clear direct bit	2	1	C2
SETB C	Set carry	1	1	D3
SETB bit	Set direct bit	2	1	D2
CPL C	Complement carry	1	1	B3
CPL bit	Complement direct bit	2	1	B2
ANL C,bit	AND direct bit to carry	2	2	82
ANL C,/bit	AND direct bit inverse to carry	2	2	B0
ORL C,bit	OR direct bit to carry	2	2	72
ORL C,/bit	OR direct bit inverse to carry	2	2	A0

MOV C,bit	Move direct bit to carry	2	1	A2
MOV bit,C	Move carry to direct bit	2	2	92
BRANCHING				
ACALL addr 11	Absolute call to subroutine	2	2	11→F1
LCALL addr 16	Long call to subroutine	3	2	12
RET	Return from subroutine	1	2	22
RETI	Return from interrupt	1	2	32
AJMP addr 11	Absolute jump unconditional	2	2	01→E1
LJMP addr 16	Long jump unconditional	3	2	02
SJMP rel	Short jump (relative address)	2	2	80
JC rel	Jump on carry = 1	2	2	40
JNC rel	Jump on carry = 0	2	2	50
JB bit,rel	Jump on direct bit = 1	3	2	20
JNB bit,rel	Jump on direct bit = 0	3	2	30
JBC bit,rel	Jump on direct bit = 1 and clear	3	2	10
JMP @A+DPTR	Jump indirect relative DPTR	1	2	73
JZ rel	Jump on accumulator = 0	2	2	60
JNZ rel	Jump on accumulator ≠ 0	2	2	70
CJNE A,dir,rel	Compare A,direct jne relative	3	2	B5
CJNE A,#d,rel	Compare A,immediate jne relative	3	2	B4
CJNE Rn,#d,rel	Compare register, immediate jne relative	3	2	B8-BF
CJNE @Ri,#d,rel	Compare indirect, immediate jne relative	3	2	B6-B7
DJNZ Rn,rel	Decrement register, jnz relative	2	2	D8-DF
DJNZ dir,rel	Decrement direct byte, jnz relative	3	2	D5
MISCELLANEOUS				
NOP	No operation	1	1	00

7.2.2 SFR

F8									FF
F0	B								F7
E8									EF
E0	ACC								E7
D8									DF
D0	PSW								D7
C8	T2CON		RCAP2L	RCAP2H	TL2	TH2			CF
C0									C7
B8	IP								BF
B0	P3								B7
A8	IE								AF
A0	P2								A7
98	SCON	SBUF							9F
90	P1			IDA	BYSY				97
88	TCON	TMOD	TLO	TL1	TH0	TH1			8F
80	P0	SP	DPL	DPH				PCON	87

7.2.3 Cache Management

BIT1628A 內建 Cache Management 用以管理 EEPROM 的資料存取。Cache Management 內包含 16 Cache Page，每一個 Cache Page Buffer 爲 256x8 bits，第一個 Cache Page 是固定定址 (Mapping to 000h~0FFh)並不會隨著 Cache update 而更新。

Cache 更新的策略爲最近最少使用(LRU, Least Recently Used)。當在程式碼執行中偵測到 Cache Page Fault，Cache Management 會從 Code Flash(EEPROM 或 Serial-Flash)中，將下一個 Page 的程式碼，搬至最近最少使用(LRU)的 Cache Page Buffer 中。

Power on Reset 後 Cache Management 會從 EEPROM 或 Serial-Flash 中，先搬移 4 個 Page 程式碼 (000h-3FFh) 至 Cache Page Buffer 中。

7.2.4 Interrupt

BIT1628A 內建 8051 MCU 的中斷服務功能，可使中斷服務的需求以中斷的方式通知 8501 MPU，以使 MPU 獨立執行主程式，而提升執行效率。在 8051 單晶片中提供 5 個中斷源，分別爲：

1. INT0：外部中斷 0。
2. Timer0：計時/計數器中斷。
3. INT1：外部中斷 1。
4. Timer1：計時/計數器中斷。
5. UART：串列埠中斷。

上列中斷源在 8051 中都有相對應的旗標，當中斷條件產生時，中斷源就會使其相對應的旗標值設定爲 1。8051 的 CPU 會在每一個機械週期檢查這些旗標的狀態，若系統允許相對的中斷源產生中斷，且該中斷相對應

的旗標值亦爲 1 時，則 CPU 會在執行完目前正在執行的指令後，將程式在記憶體中的位址存入堆疊中，並產生中斷服務副程式的呼叫，跳到該中斷所對應之中斷向量位址去執行，CPU 執行該中斷服務副程式，直到「RETI」指令後才結束中斷副程式，再從堆疊中取出先前存入的位址值繼續執行被中斷的程式。

7.2.4.1 8051 的中斷向量與中斷相關暫存器

BIT1628A 內建 8051 MCU 的 5 個中斷源，其中斷向量、旗標名稱與該旗標所屬暫存器如下：

中斷致能暫存器結構：位址：A8H

EA	----	----	ES	ET1	EX1	ET0	EX0

中斷優先暫存器(Interrupt Priority register，可位先定址)，其結構如下：位址：B8H

----	----	----	PS	PT1	PX1	PT0	PX0

中斷源	中斷向量
Reset	0000H
$\overline{INT0}$	0003H
Timer0	000BH
$\overline{INT0}$	0013H
Timer1	001BH
UART	0023H

7.2.5 GPIO

BIT1628A 內建 8051 MCU 具有 3 個 8 位元(bits)的輸出輸入埠，經由這三個輸出輸入埠與外界進行資料交換因此在 8051 內部用個暫存器來記錄輸出/輸入接腳的狀態，分別爲資料記憶體 80h、90h、A0h 等三個位元組(byte)，並依輸出/輸入埠分別命名爲 P0、P1、P2。當軟體程式對輸出輸入埠 P0～2 作輸出/輸入的動作，即是對 80h、90h、A0h 等三個位元組作寫入/讀出的動作。

BIT1628A GPIO 採用 Multi-Function Pin Definition 因此需設定相關 register，相關設定如下表

Table 7-2 GPIO and UART Register

Mnemonic	Address	R/W	Bits	Description	Default
R_UART_SRC	0x18F[3:2]	RW	2	UART source select	0
				UART Function Enable 0: Disable 1: Enable	0
R_BIN_GPIO	0x18F[4]	RW	1	P2 Mapping to BIN Port	0

R_GIN_GPIO	0x18F[5]	RW	1	P1 Mapping to GIN Port	0
R_RIN_GPIO	0x18F[6]	RW	1	P0Mapping to RIN Port 0: Disable 1: Enable	0

7.2.6 Timer

BIT1628A 內建 8051 MCU 的內部有 3 個計時/計數器，可接收外界輸入的驅動信號，而能產生一個輸出信號以供讀取外界輸入信號發生的次數。如果這個外界輸入信號代表某一事件發生的次數，則計時/計數器即是在作事件的計數；如果這個外界輸入信號是一個固定頻率的信號，則計時/計數器則可用以作計算時間的工作。

7.2.6.1 計時/計數器的驅動與使用

Timer0 與 Timer1 是 8051MCU 的兩個 16 位元計時/計數器，其計數值是存放於兩個 8 位元暫存器中，Timer0 的計數是由 TH0(High byte)及 TL0(Low byte)來執行，Timer1 的計數是由 TH1(High byte)及 TL1(Low byte)來執行。其位址分別位於 SFR 內部記憶體的 8Ch、8Ah、8Dh 及 8Bh 中。

在使用 8051MCU 計時/計數器前須先設定計時/計數器模式控制暫存器(Timer/counter Mode Control Register，簡稱 TMOD)及計時/計數器控制暫存器(Timer/counter Control Register，簡稱 TCON)兩個暫存器，此二暫存器分別用來決定 Timer0 及 Timer1 的工作模式及中斷執行的控制設定。

7.2.6.2 TMOD 模式控制暫存器之設定

Timer 的計時時脈來源有兩種，一種是 8051MCU 的內部時脈，一種是 BIT1628A 內所設定的 Timer 來源(OVSYNC、OHSYNC、IHSYNC 或 External Pin)所輸入的外部時脈。在 8051MCU 接收時脈計時/計數時，會在每個 Falling Edge 時，將 Timer 的值累加 1。而 8051MCU 對時脈來源的選擇是由 TMOD 暫存器中的 C/T 位元來決定。當 C/T 設定爲 1 時，Timer 使用外部時脈；當 C/T 設定爲 0 時，Timer 使用內部時脈。TMOD 的結構如下：

GATE	C / T	M1	M0	GATE	C / T	M1	M0

7.2.6.3 TCON 控制暫存器之設定

TCON 爲 Timer 的計時控制暫存器，其結構如下

TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

7.2.7 UART

BIT1628A 內建之 8051 MCU 的串列埠是一組全雙工的 UART，即 8051 的 UART 可以在同一時間進行串列資料的傳送與接收。BIT1628A 內建之 8051 MCU 使用 HSYNC 接腳做爲串列傳輸的接收端(RxD)，.VSYNC 接腳做爲串列傳輸的輸出端(TxD)，並利用特殊功能暫存器(Special Function Register，簡稱 SFR)中的串列埠緩衝器(Serial Port Buffer，簡稱 SBUF)執行串列傳輸的工作。當串列傳輸工作設定完成之後，傳送端會存入一筆資料到 SBUF 中，並藉以引發資料傳送的動作；當串列傳輸工作設定完成之後，接收端會將接收資料放入 SBUF 中。但在 8051 單晶片的 UART 結構中，接收資料端與傳送資料端實際使用的暫存器並不是同一個，只不過它們均對應到相同的定址位址，因此在傳送或接收資料時，8051 單晶片會自動選擇使用不同的暫存器，所以 8051 的串列埠可以同時進行資料的傳送與接收。

BIT1628A 內建之 8051 MCU 進行串列資料傳輸時，串列埠具有輸入緩衝的功能，即當串列埠接收到一筆資料後，會把資料存放至 SBUF 中，然後繼續接收資料，並在接收或等待接收下一筆資料的過程中處理 SBUF 中的資料。因此，串列埠可以持續不斷的接收資料，而不必在接收一筆資料後等待該資料完全處理完畢才進行下一筆資料的接收。但在第二筆資料被 UART 接收完畢前，第一筆資料須被處理完畢由程式讀入，否則會產生資料流失的問題。

7.2.7.1 UART 相關暫存器

在 SFR 記憶體中與 UART 相關的暫存器有兩個，分別爲串列埠控制暫存器(Serial Port Control register，簡稱爲 SCON)及電源控制暫存器(Power Control register，簡稱爲 PCON)。以下爲此二暫存器的結構圖：

SCON：串列埠控制暫存器 (SERIAL PORT CONTROL REGISTER) 位址：98h

SM0	SM1	SM2	REN	TB8	RB8	TI	RI

PCON：電源控制暫存器 (POWER CONTROLREGISTER) 位址：(87h)

SMOD	—	—	—	GF1	GF0	PD	IDL

7.2.8 External Memory

BIT1628A 內建 8051MCU 透過 External Memory Interface 存取 BIT1628A 內建之 Register，8051 External Memory 0000h~07FFh，對應至 BIT1628A Slave Mode Interface Address 000h ~ 7FFh。

7.2.9 Debug Mode

BIT1628A 內建之 8051 MCU 提供兩組硬體中斷(break point)，Debug Mode 啓動後，當 8051 內部程式計數器(PC)執行到所設定的兩組硬體中斷的中斷位址相同時，將會使 8051 進入 Hold 的狀態，並且自動將 Interface Mode 切換爲 Slave Mode，此時可以透過 Two-Wire Serial Interface (TWSI)，將 IC 內的 register 和 8051 Internal Memory 的數值讀出，然再將 R_M8051_RELEASE 設爲 1，回到 Master Mode，此時 8051 將會從上一次 Break Point 的位置再往下繼續執行。相關設定如下

Table 7-3 M8051 Break Register

Mnemonic	Address	R/W	Bits	Description	Default
R_M8051_BREAK1	0x18B[7:0],0x18A[7:0]	RW	16	M8051 Break Point 1	0xFFFF
R_M8051_BREAK2	0x18D[7:0],0x18C[7:0]	RW	16	M8051 Break Point 2	0xFFFF

R_M8051_RELEASE	0x18E[0]	RW	1	M8051 Debug Release 0: Disable 1: Enable	0
R_M8051_DEBUG	0x18E[1]	RW	1	M8051 Debug Mode 0: Disable 1: Enable	0

7.3 Slave Mode

BIT1628A 提供 Two-Wire Serial Interface (TWSI) Protocol 來存取 Register Sets，並由 OP4~OP2 來設定所對應的 Slave Address。

7.3.1 TWSI Protocol Device Address

BIT1628A TWSI Protocol 須在送出 Start Bit 之後送出 8 Bits Device Address (slave address)，並可由外部 PIN (OP4、OP3 和 OP2)決定其 Device Address 的 Bit6 和 Bit5 位址。

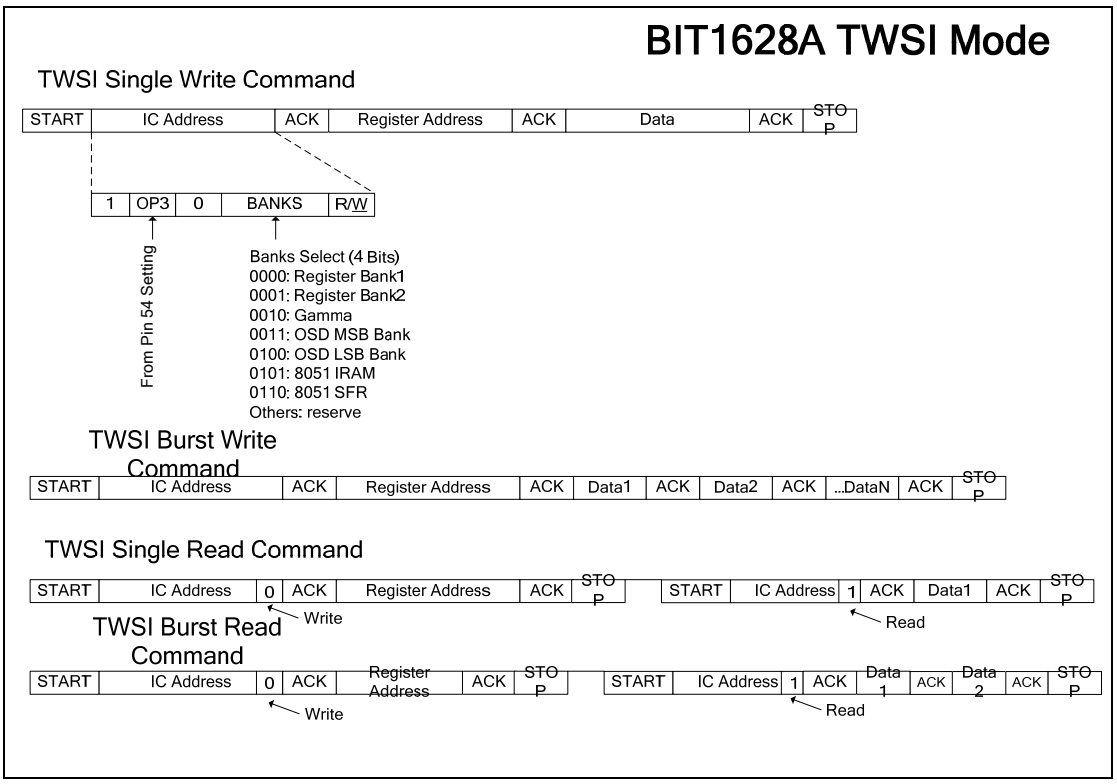
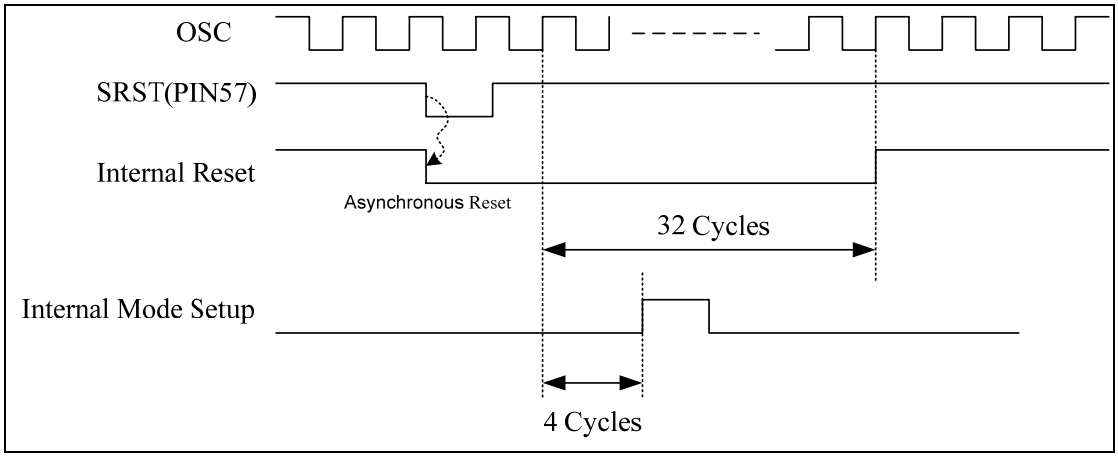


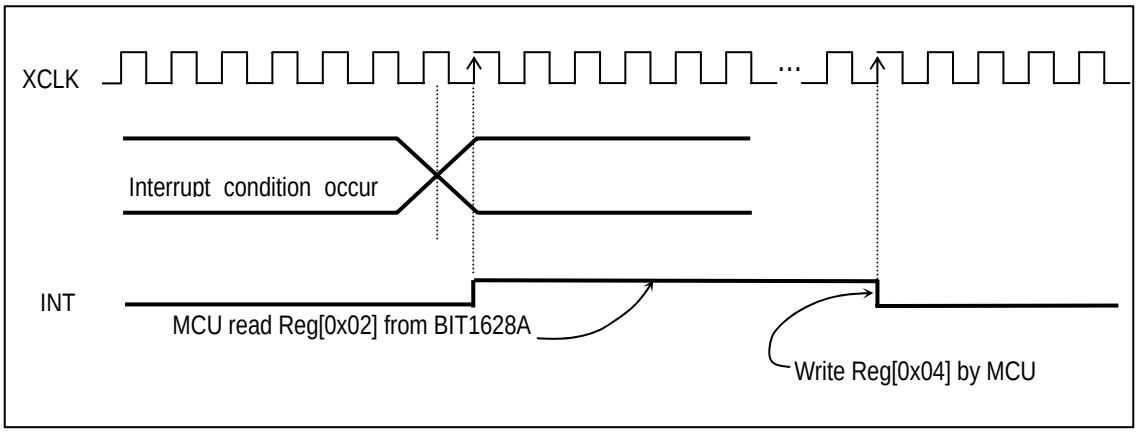
Figure 7-1 TWSI Read/Write Mode

8 Timing Diagram

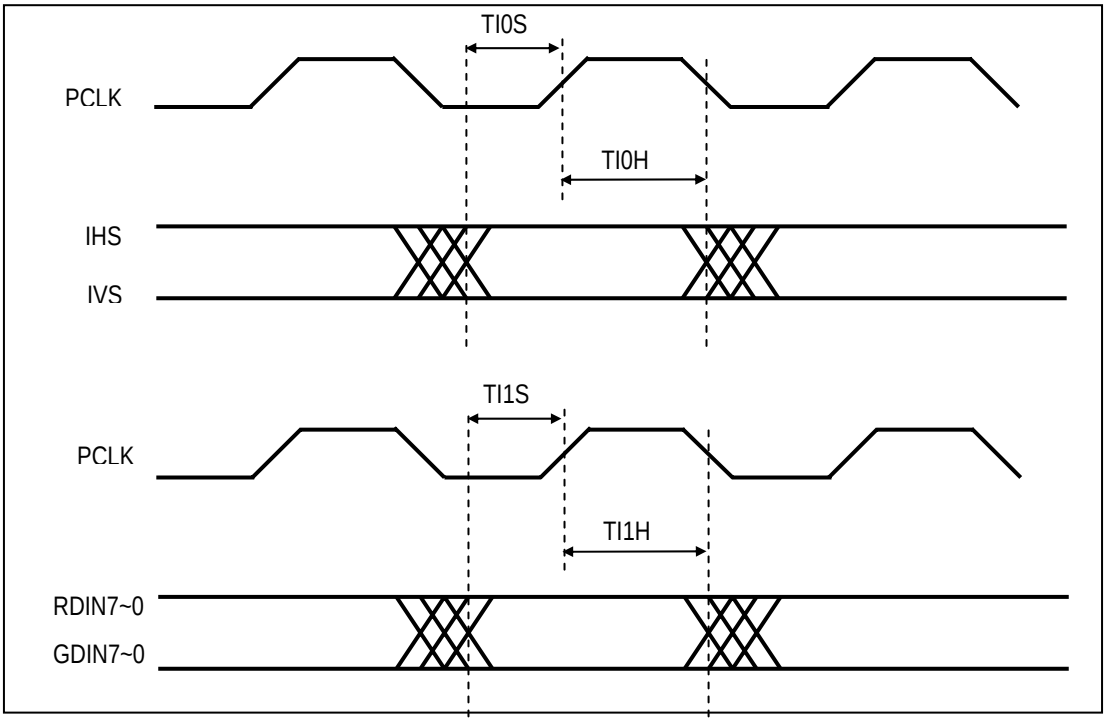
8-1 Hardware Reset:



8-2 Clock and Interrupt:

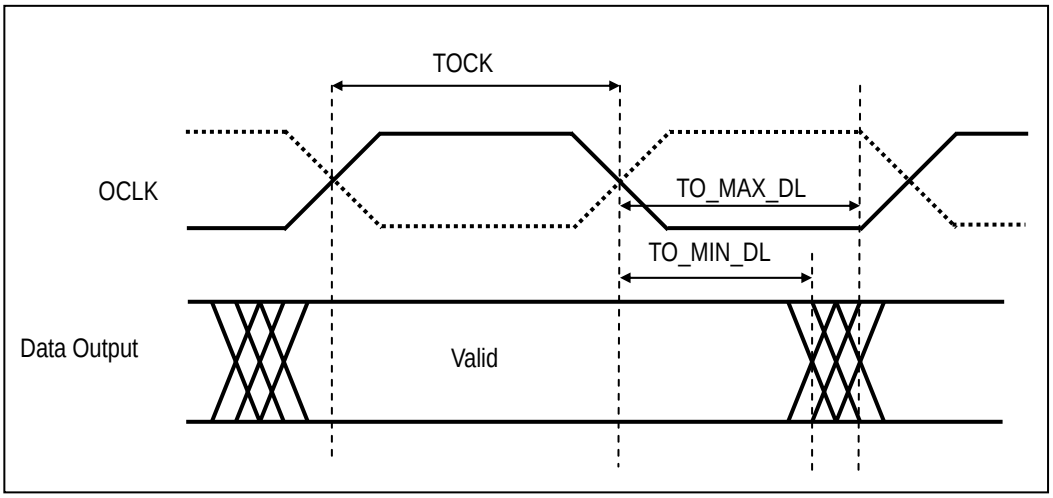


8-3 Input Signal:



Symbol	Describe	Max.	Min.	Unit
TI0S,TI1S	Input Setup time		2	Ns
TI0H,TI1H	Input Hold time		2	Ns

8-4 Output Signal:



Symbol	Describe	Timing	Unit
TOCK	Output clock half period		ns
TO_MAX_DL	Output signal Max delay	TOCK - 1	ns
TO_MIN_DL	Output signal Min delay	TOCK - 4	ns

9 Electrical Characteristic

9-1 Absolute Maximum Rating

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
AVDD	Supply Voltage for Analog Core	-0.5		3.6	V
VDD18	Supply Voltage for Digital Core	- 0.5		2.5	V
V_{IN}	Input Voltage for Digital Core (5V Tolerant)	- 0.5		6	V
T_{STG}	Storage Temperature	- 40		125	℃

9-2 Recommend Operating Condition

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
AVDD	Supply Voltage for Analog Core	3.0	3.3	3.6	V
VDD18	Supply Voltage for Digital Core	1.62	1.8	1.98	V
VDD33	Supply Voltage for I/O Pad	3.0	3.3	3.6	V
T_{OPR}	Operating Temperature	0		70	℃

9-3 DC Electrical Characters

(under Recommend Operating Condition and T_J =0℃ to 115℃)

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
I_{IL}	Input Leakage Current	No pull-up nor pull-down			10	uA
I_{OZ}	Tri-state Leakage Current				10	uA
V_{IL}	Input Low Voltage	CMOS	-0.3		0.8	V
V_{IH}	Input High Voltage	CMOS	2.0		5.5	V
V_{OL}	Output Low Voltage	I_{OL}= 4,8,16 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH}= 4,8, 16 mA	2.4			V
Vt-	Schmitt trigger negative going threshold voltage	CMOS	0.89	0.94	0.99	V
Vt+	Schmitt trigger positive going threshold voltage	CMOS	1.44	1.50	1.56	V
Rpu	Pull-up Resistance		39	65	116	KΩ
Rpd	Pull-down Resistance		40	56	108	KΩ

Note: The capacitance listed above does not include pad capacitance and package capacitance. One can estimate pin capacitance by adding pad capacitance about 0.5pF and the package capacitance.

10 Soldering Information

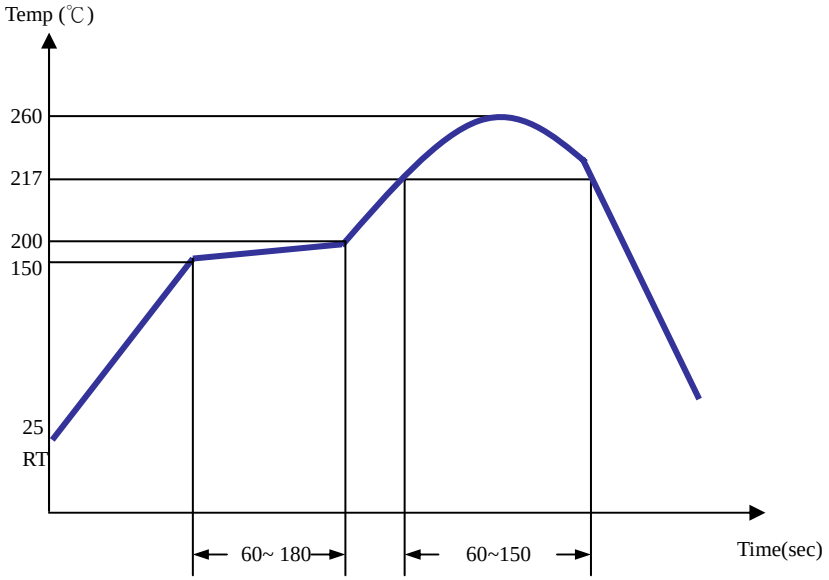
10-1 Reflow Soldering

The choice of heating method may be influenced by plastic QFP package). If infrared or vapor phase heating is used and the package is not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stenciling or pressure-syringe dispensing before package placement. Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferable be kept below 245 °C for thick/large packages (packages with a thickness ≧ 2.5 mm or with a volume ≧ 350 mm^3 so called thick/large packages). The top-surface temperature of the packages should preferable be kept below 260 °C for thin/small packages (packages with a thickness < 2.5 mm and a volume < 350 mm^3 so called thin/small packages).

Stage	Condition	Duration
1'st Ram Up Rate	max3.0+/-2℃/sec	-
Preheat	150℃~200℃	60~180 sec
2'nd Ram Up	max3.0+/-2℃/sec	-
Solder Joint	217℃ above	60~150 sec
Peak Temp	260 +0/-5℃	20~40 sec
Ram Down rate	6℃/sec max	-



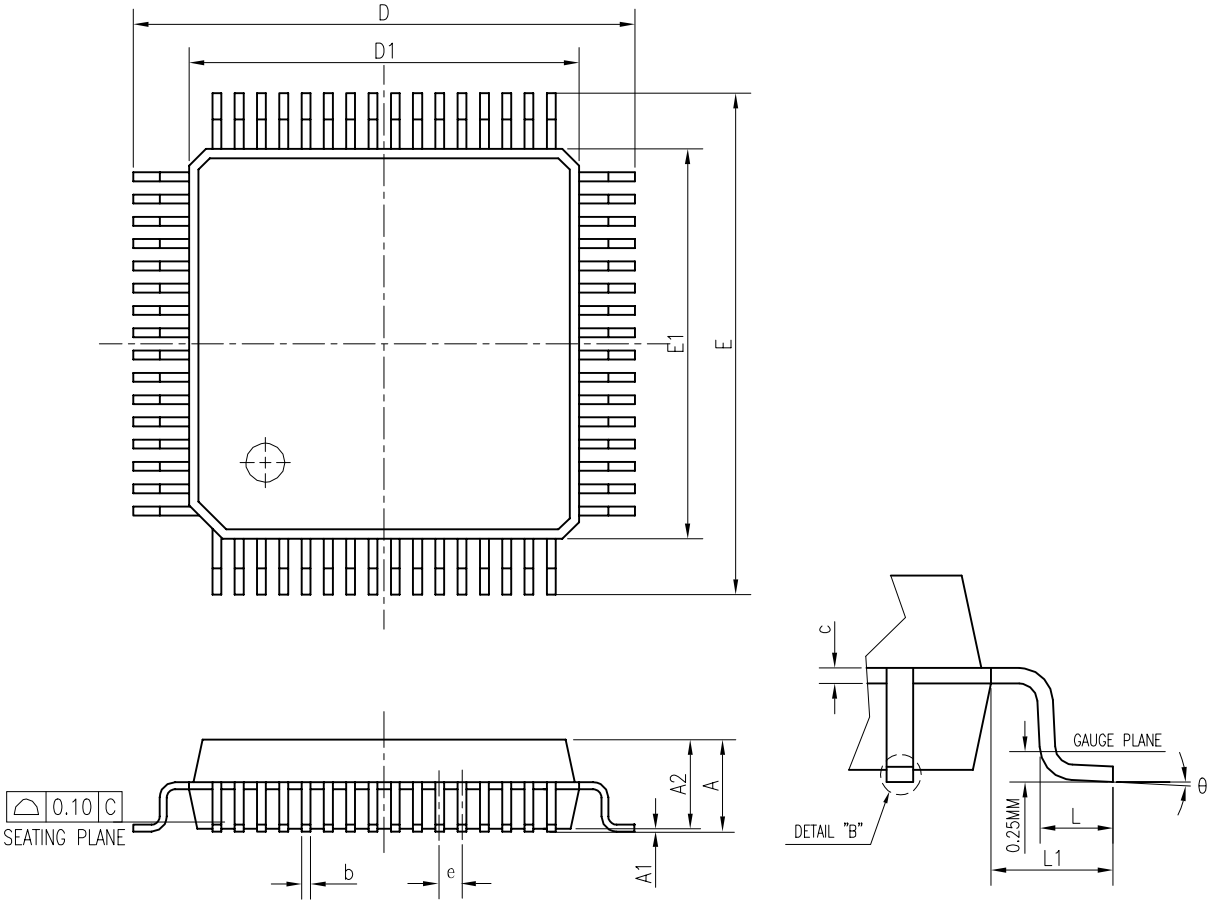
10-2 Wave Soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

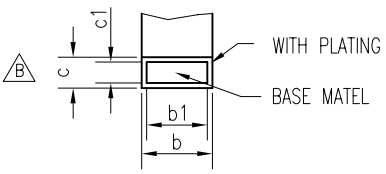
10-3 Manual Soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

11 Package Information



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	8.90	9.00	9.10	0.350	0.354	0.358
D1	6.90	7.00	7.10	0.272	0.276	0.280
E	8.90	9.00	9.10	0.350	0.354	0.358
E1	6.90	7.00	7.10	0.272	0.276	0.280
B c	0.178 TYP.			0.007 TYP.		
c1	0.127 TYP.			0.005 TYP.		
L	0.50	0.60	0.70	0.020	0.024	0.028
L1	1.00 REF.			0.039 REF.		
θ	0	3.5	7	0	3.5	7
JEDEC						



DETAIL "B"

	b (MM)			b1 (MM)			e (MM)			JEDEC
N	MIN.	NOM	MAX.	MIN.	NOM	MAX.	MIN.	NOM	MAX.	
64L	0.13	0.18	0.23	0.13	0.16	0.19	0.40 BSC.			MS-026 BBD